INTEGRATED CIRCUITS

DATA HANDBOOK

Advanced CMOS logic
ACL

BOOK IC07 1989

Philips Components

PHILIPS

ADVANCED CMOS LOGIC ACL

page

Preface iii
Product status iv
Contents v

Section 1 – Introduction
Introduction 1-3
Numeric index 1-8
Functional index 1-10
Ordering information 1-14

Section 2 – Quality and Reliability
Quality and Reliability 2-3

Section 3 – Family Characteristics
Family Specifications 3-3
Data Sheet Specification Guide 3-6
Definitions and Symbols 3-8

Section 4 – ACL Pinouts
ACL Pinouts 4-3

Section 5 – ACL Data Sheets
Data Sheets 5-3

Section 6 – Application Notes
Index 6-1

Section 7 – Packaging Information
Package outlines 7-3

Signetics reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Signetics assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Signetics makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS

Signetics' Products are not designed for use in life support appliances, devices, or systems where malfunction of a Signetics Product can reasonably be expected to result in a personal injury. Signetics' customers using or selling Signetics' Products for use in such applications do so at their own risk and agree to fully indemnify Signetics for any damages resulting in such improper use or sale.

Signetics registers eligible circuits under the Semiconductor Chip Protection Act.

© Copyright 1988 Signetics Corporation

All rights reserved.

Preface

Signetics would like to thank you for your interest in our ACL product family. Utilizing a 1μm CMOS process, Signetics' ACL has joined the lowest power-delay product family in the market today. This, coupled with its standard setting, low-noise, system reliable pinout, makes it an obvious favorite among system designers.

In addition to ACL, Signetics Standard Products Division offers the industry's broadest line of commercially available logic products. These products span a wide speed/power spectrum from 100K/10K ECL, to FAST to 74HC/HCT and other industry standard families such as: the CMOS 4000B series, 74, 74LS, 74S, 8T, and 8200 Logic. Information regarding these products lines is also available from your nearest Signetics Sales Office, sales representative, or authorized distributor.

Standard Products Division

Product Status

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains a preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible products.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Contents

Preface iii

Product Status iv

Section 1 - Introduction
- **Introduction** 1-3
- **Numeric Index** 1-8
- **Functional Index** 1-10
- **Ordering Information** 1-14

Section 2 - Quality And Reliability
- **Quality and Reliability** 2-3

Section 3 - Family Characteristics
- **Family Specification** 3-3
- **Data Sheet Specification Guide** 3-6
- **Definitions and Symbols** 3-8

Section 4 - ACL Pinouts

Section 5 - ACL Data Sheets

74AC/ACT11000	Quad 2-Input NAND Gate	5-3
74AC/ACT11002	Quad 2-Input NOR Gate	5-7
74AC/ACT11004	Hex Inverter	5-11
74AC/ACT11008	Quad 2-Input AND Gate	5-15
74AC/ACT11010	Triple 3-Input NAND Gate	5-19
74AC/ACT11011	Triple 3-Input AND Gate	5-23
74AC/ACT11013	Dual 4-Input NAND Schmitt-Trigger	5-27
74AC/ACT11014	Hex Inverter Schmitt-Trigger	5-31
74AC/ACT11020	Dual 4-Input NAND Gate	5-35
74AC/ACT11021	Dual 4-Input AND Gate	5-39
74AC/ACT11027	Triple 3-Input NOR Gate	5-43
74AC/ACT11030	8-Input NAND Gate	5-47
74AC/ACT11032	Quad 2-Input OR Gate	5-51
74AC/ACT11034	Hex Non-Inverter	5-55
74AC/ACT11074	Dual D-Type Flip-Flop w/Set and Reset; Positive-Edge Trigger	5-59
74AC/ACT11086	Quad 2-Input Exclusive-OR Gate	5-66
74AC/ACT11109	Dual J-K Flip-Flop w/Set and Reset; Positive-Edge Trigger	5-70
74AC/ACT11112	Dual J-K Flip-Flop w/Set and Reset; Negative-Edge Trigger	5-77
74AC/ACT11132	Quad 2-Input NAND Schmitt-Trigger	5-84
74AC/ACT11138	3-to-8 Line Decoder/Demultiplexer; Active-Low	5-88
74AC/ACT11139	Dual 2-to-4 Line Decoder/Demultiplexer; Active-Low	†
74AC/ACT11151	8-Input Multiplexer	5-94
74AC/ACT11153	Dual 4-Input Multiplexer	†
74AC/ACT11157	Quad 2-Input Multiplexer	†
74AC/ACT11158	Quad 2-Input Multiplexer, INV	5-100
74AC/ACT11160	Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset	5-105
74AC/ACT11161	Synchronous Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset	†
74AC/ACT11162	Synchronous Presettable Synchronous BCD Decade Counter; Synchronous Reset	5-115
74AC/ACT11163	Synchronous Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset	†
74AC/ACT11168	Synchronous Up/Down BCD Decade Counter	†
74AC/ACT11169	Synchronous Presettable 4-Bit Up/Down Binary Decade Counter	†

† For more information on these devices contact your local sales organization; see addresses on back cover.

Contents

74AC/ACT11174	Hex D-Type Flip-Flop w/Reset; Positive-Edge Trigger	†
74AC/ACT11175	Quad D-Type Flip-Flop w/Reset; Positive-Edge Trigger	5-124
74AC/ACT11181	4-Bit Arithmetic Logic Unit	†
74AC/ACT11190	Asynchronous Presettable Synchronous Decade Up/Down Counter w/Single Clock	5-131
74AC/ACT11191	Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Single Clock	5-142
74AC/ACT11192	Asynchronous Presettable Synchronous BCD Decade Up/Down Counter w/Dual Clock	†
74AC/ACT11193	Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Dual Clock	†
74AC/ACT11194	4-Bit Bidirectional Universal Shift Register	5-153
74AC/ACT11238	3-to-8 Line Decoder/Demultiplexer; Active-High	5-161
74AC/ACT11239	Dual 2-to-4 Line Decoder/Demultiplexer; Active-High	†
74AC/ACT11240	Octal Buffer/Line Driver, INV (3-State)	5-167
74AC/ACT11241	Octal Buffer/Line Driver (3-State)	5-171
74AC/ACT11244	Octal Buffer/Line Driver (3-State)	5-175
74AC/ACT11245	Octal Transceiver w/Direction Pin (3-State)	5-179
74AC/ACT11251	8-Input Multiplexer (3-State)	5-183
74AC/ACT11253	Dual 4-Input Multiplexer (3-State)	5-189
74AC/ACT11257	Quad 2-Input Multiplexer (3-State)	5-195
74AC/ACT11258	Quad 2-Input Multiplexer, INV (3-State)	5-201
74AC/ACT11269	Synchronous Presettable 8-Bit Binary Up/Down Counter	†
74AC/ACT11280	9-Bit Odd/Even Parity Generator/Checker	5-207
74AC/ACT11286	9-Bit Odd/Even Parity Generator/Checker w/Bus Drive I/O Port	5-212
74AC/ACT11299	8-Input Universal Shift/Storage Register w/Asynchronous Reset and Common I/O Pins	†
74AC/ACT11323	8-Input Universal Shift/Storage Register w/Synchronous Reset and Common I/O Pins	†
74AC/ACT11352	Dual 4-Input Multiplexer, INV	†
74AC/ACT11353	Dual 4-Input Multiplexer, INV (3-State)	5-218
74AC/ACT11373	Octal D-Type Transparent Latch (3-State)	5-224
74AC/ACT11374	Octal D-Type Flip-Flop; Positive-Edge Trigger (3-State)	5-231
74AC/ACT11378	Hex D-Type Flip-Flop w/Enable; Positive-Edge Trigger	†
74AC/ACT11379	Quad D-Type Flip-Flop w/Data Enable	†
74AC/ACT11520	8-Bit Identity Comparator w/Input Pull-Up	5-237
74AC/ACT11521	8-Bit Identity Comparator	5-242
74AC/ACT11533	Octal D-Type Transparent Latch, INV (3-State)	5-247
74AC/ACT11534	Octal D-Type Flip-Flop; Positive-Edge Trigger, INV (3-State)	5-254
74AC/ACT11568	Synch. Presettable BCD Decade Up/Down Counter w/Synch. and Asynch. Reset	†
74AC/ACT11569	Synch. Presettable 4-Bit Binary Up/Down Counter w/Synch. and Asynch. Reset	†
74AC/ACT11579	8-Bit Binary Up/Down Counter w/Common I/O Pins; Synch. and Asynch. Reset (3-State)	†
74AC/ACT11620	Octal Transceiver w/Dual Enable, INV (3-State)	†
74AC/ACT11623	Octal Transceiver w/Dual Enable (3-State)	†
74AC/ACT11640	Octal Transceiver w/Direction Pin, INV (3-State)	5-260
74AC/ACT11643	Octal Transceiver (3-State); True/INV	†
74AC/ACT11646	Octal Transceiver/Register w/Direction Pin (3-State)	†
74AC/ACT11648	Octal Transceiver/Register w/Direction Pin, INV (3-State)	†
74AC/ACT11651	Octal Transceiver/Register w/Dual Enable, INV (3-State)	†
74AC/ACT11652	Octal Transceiver/Register w/Dual Enable (3-State)	†
74AC/ACT11657	Octal Transceiver w/8-Bit Parity Checker/Generator	†
74AC/ACT11810	Quad 2-Input Exclusive-NOR Gate	5-264
74AC/ACT11818	8-Bit Diagnostic/Pipe-Line Register	†
74AC/ACT11819	8-Bit Diagnostic/Pipe-Line Register w/Parity Even Output	†
74AC/ACT11821	10-Wide D-Type Flip-Flop; Positive-Edge Trigger (3-State)	†
74AC/ACT11822	10-Wide D-Type Flip-Flop; Positive-Edge Trigger (3-State), INV	†
74AC/ACT11823	9-Wide D-Type Flip-Flop w/Reset and Enable; Positive-Edge Trigger (3-State)	†
74AC/ACT11824	9-Wide D-Type Flip-Flip w/Reset and Enable; Positive-Edge Trigger, INV (3-State)	†
74AC/ACT11825	Octal D-Type Flip-Flop w/Reset and Enable; Positive-Edge Trigger (3-State)	†
74AC/ACT11826	Octal D-Type Flip-Flop w/Reset and Enable; Positive-Edge Trigger, INV (3-State)	†
74AC/ACT11827	10-Wide Buffer/Line Driver (3-State)	†
74AC/ACT11828	10-Wide Buffer/Line Driver, INV (3-State)	†
74AC/ACT11833	8-Bit Transceiver w/9-Bit Parity Checker/Generator and Error Flip-Flop	†
74AC/ACT11834	8-Bit, INV Transceiver w/9-Bit Parity Checker/Generator and Error Flip-Flop	†

† For more information on these devices contact your local sales organization; see addresses on back cover.

Contents

74AC/ACT11841 10-Wide D-Type Transparent Latch (3-State) ..... †
74AC/ACT11842 10-Wide D-Type Transparent Latch, INV (3-State) ..... †
74AC/ACT11843 9-Wide D-Type Transparent Latch w/Set and Reset (3-State) ..... †
74AC/ACT11844 9-Wide D-Type Transparent Latch w/Set and Reset, INV (3-State) ..... †
74AC/ACT11845 Octal D-Type Transparent Latch w/Set and Reset (3-State) ..... †
74AC/ACT11846 Octal D-Type Transparent Latch w/Set and Reset, INV (3-State) ..... †
74AC/ACT11853 8-Bit Transceiver w/9-Bit Parity Checker/Generator and Error Flag Latch ..... †
74AC/ACT11854 8-Bit INV Transceiver with 9-Bit Parity Checker/Generator and Error Flag Latch ..... †
74AC/ACT11861 10-Wide Transceiver (3-State) ..... †
74AC/ACT11862 10-Wide Transceiver (3-State), INV ..... †
74AC/ACT11863 9-Wide Transceiver: 3-State ..... †
74AC/ACT11864 9-Wide Transceiver, INV (3-State) ..... †
74AC/ACT11873 Dual D-Type 4-Bit Transparent Latch w/Reset (3-State) ..... †
74AC/ACT11874 Dual D-Type 4-Bit Flip-Flop Latch w/Reset (3-State) ..... †
74AC/ACT11881 4-Bit Arithmetic Logic Unit w/Status Check Register ..... †
74AC/ACT11882 32-Bit Look-Ahead Carry Generator ..... †
74AC/ACT11898 10-Bit Serial-In Parallel-Out Shift Register 5-268

Section 6 - Application Notes

AN600 Handling Procedures 6-3
AN606 Simultaneous Switching Evaluation of Advanced CMOS Logic 6-5
AN203 Test Fixtures for High-Speed Logic 6-9

Section 7 - Packaging Information

Packaging Information 7-3

† For more information on these devices contact your local sales organization; see addresses on back cover.

Section 1
Introduction

INDEX

Introduction 1-3
Numeric Index 1-8
Functional Index 1-10
Ordering Information 1-14

Introduction

INTRODUCTION

There is little doubt that CMOS is closing in on bipolar technology as the mainstay of integrated commodity logic. Advancing technology is rapidly eliminating the old trade-offs between speed and power dissipation (see Figure 1), and problems peculiar to CMOS such as latch-up and ESD sensitivity have already been solved. However, until now, CMOS logic ICs have been unable to match the high speed and the high current output of TTL technologies which is essential for operation in the bus or transmission line environment of the fastest logic systems.

The introduction of the Advanced CMOS Logic (ACL) family of ICs removes this hurdle. Signetics fabricates ACL in a 1-micron twin-well CMOS process with recessed local oxidation and a titanium disilicide layer on the gate, source and drain areas to reduce the contact and interconnect resistance. This, together with oxidation of the gate sidewalls for reduced capacitance, leads to increased drive and speed that equals that of the fastest bipolar TTL logic. With an average propagation delay of 5ns (150MHz operation) and 24mA sink/source capability, ACL supplements the HE4000B and HCMOC IC ranges to allow designers to implement the outstanding CMOS benefits of wide and symmetrical noise margins, high reliability, and reduced power dissipation across the whole speed spectrum of logic circuitry.

The inevitable fast edges associated with the exceptionally high speed of ACL required one final hurdle to be removed: the problem, which also exists for fast-switching bipolar logic, can reduce system noise margins, cause loss of stored data and reduce system speed. We have solved it for ACL by discarding the traditional corner supply pinning arrangement and simultaneously adopting a flowthrough architecture wherein the supply pins are at the center of each side of the package (where the internal inductance is minimum), all the input pins are on one side, all the output pins are on the other, and control pins are at the corners. Although this solution means that ACL is not pin-compatible with the comparable TTL and HCMOS functions, as an engineering-driven company, we felt that the considerations of improving system reliability, simplifying pcb design and reducing board area should take precedence.

All types within our ACL family have outputs that are both CMOS and TTL-compatible and are available for operating temperature ranges of -40°C to +85°C (commercial/industrial: 74AC/ACT prefix) or -55°C to +125°C (military: 54AC/ACT prefix). They come in two versions:

- Fully buffered 54/74AC types with CMOS-compatible input switching levels (typically $V_{CC}/2$) and a supply voltage range of 3V to 5.5V for all-CMOS systems
- Fully buffered 54/74ACT types with TTL-compatible input switching levels (typically 1.5V) and a supply voltage range of 5V±10% for interfacing with TTL systems

Since the low power dissipation of our ACL ICs makes them ideal for circuitry on densely packed boards in small enclosures, we didn't overlook the need to make them compatible with surface mounting technology which is being increasingly used for automated assembly of electronic equipment to achieve significant reduction of its size and weight. Production quantities of *all* our ACL ICs are available in DIP packages and in SO (small outline) packages. The dimensions of the latter were originally developed by us and now form the basis of JEDEC standard publication 95 (also published in IEC standard document 191-2, family A76).

ACL ICs are completely latch-up free and have complete protection against electrostatic discharge (ESD) at their inputs.

ACL IN A NUTSHELL

ACL has all the well-known attributes of our HCMOS family combined with faster operation and increased drive capability. Here are 14 reasons why Signetics is head and shoulders above the rest:

- A comprehensive type range from simple gates to shift registers and counters
- All types available in 74AC versions (CMOS input levels) and 74ACT versions (TTL input levels)
- All types available in SO (small outline) packages as well as in DIP, so you can use surface-mount techniques to increase pcb packing density. The 14 and 16-pin SO packages are the narrower 150mil (3.8mm) versions and are available on 16mm tape on 13 inch diameters reels (2500 ICs). The 16, 20, 24 and 28-pin SO packages are 300mil (7.6mm) wide and are available on 24mm tape with 1000 ICs on a 13 inch reel. The body width of all the DIP packages (14 to 28 pins) is 300mil (7.6mm).
- Completely latch-up free and fully ESD protected up to ±2kV (human body model) at all inputs and outputs.
- Low power dissipation. Typical quiescent current per package is only a few nanoamps for gates, flip-flops and MSI. Typical counter operating current with a 5V supply is 250µA at 1MHz and increases linearly with frequency.
- 24mA sink/source current. For incident wave switching 74AC/ACT types can provide ±75mA (for driving a 50Ω load).
- ACL input current is only 1µA in the High or Low state. This is essentially zero compared with the input current of TTL technologies. The fan-out to other CMOS ICs is therefore only limited by load capacitance considerations and not by DC loads.
- More than three times the noise immunity of TTL. Input switching levels are between 30% and 70% of V_{CC} for 74AC types and between 0.8V and 2V for 74ACT types. The output swing for all ACL ICs is from 0.1V to V_{CC}-0.1V with a load of 50µA (fifty ACL inputs), and from 0.5V to V_{CC}-0.8V with a load of ±24mA.
- The input switching threshold level is subject to a variation of only ±60mV over the entire temperature range, much less than the ±300mV

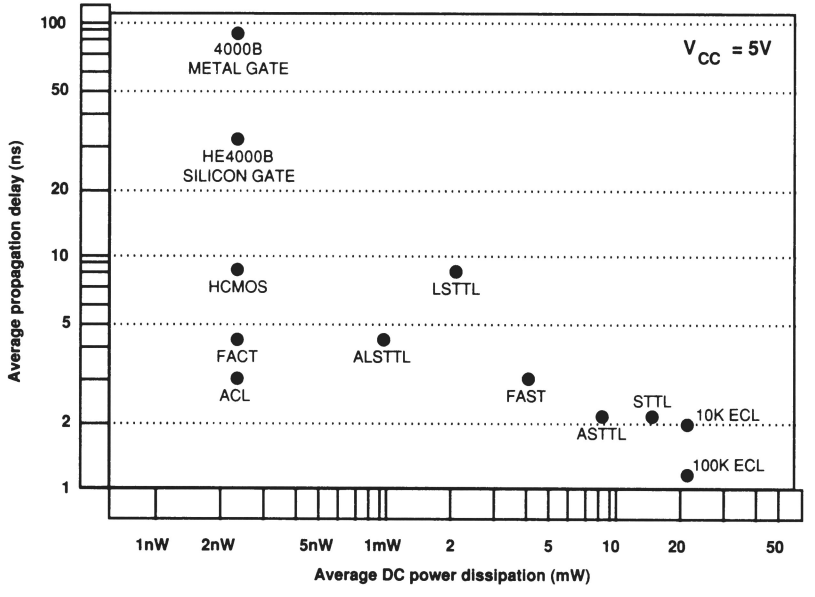


Figure 1. The Logic Family Speed/Power Sectrum

specified for advanced TTL families.

- Wide supply voltage range. AC versions are specified with a supply from 3V to 5.5V (the internal logic state is maintained down to 2V). Battery back-up is no problem and automotive applications are possible. TTl-compatible ACT versions are specified with a supply of 5V ± 10%.
- With a 5V supply, average propagation delay for a gate is 5ns for either High-to-Low or Low-to-High transitions into a capacitive load of 50pF. On-chip propagation delay for gates is only 0.5ns. Typical operating frequency is up to 150MHz at 25°C and f_{MAX} is simply specified with a 50% duty factor.
- Outputs have edge control circuits to reduce the effective dv/dt, thereby further reducing switching noise. The output buffers are standardized to allow symmetrical output current sourcing and sinking for equal output rise and fall times. This results in simplified design combined with optimum speed and AC performance.
- Center supply pins and flowthrough architecture to minimize ground and supply rail glitches during simultaneous switching of outputs, and to simplify board layout.
- All ACL critical inputs have a new patented dynamic hysteresis to make them less susceptible to slow input edges. (A critical input is considered an input which controls more than one output.)
- Extensive customer support is available.
- Signetics ACL ICs are alternate-source by TI.

A CLOSER LOOK AT ACL

Supply Voltage

ACL circuits with the type number prefix 74AC operate from a supply voltage range of 3V to 5.5V which meets the new industry JEDEC standard No. 8 which specifies 3.3V ±0.3V for regulated power supply systems. The internal logic of 74AC circuits will, however, maintain its state with a supply voltage as low as 2V. This facilitates the use of a lithium battery as a back-up supply. ACL circuits with the type number prefix 74ACT operate from a supply voltage of 5V ±10% which is consistent with the supply voltage for the TTL logic circuits with which they are intended to interface.

Power Dissipation

One of the most important requirements for any logic system is low power dissipation because it minimizes system cost, allows higher packing density, and results in improved reliability because of lower operating temperature.

The typical quiescent power dissipation of an ACL gate (2.5nW) is more than six orders of magnitude less than that of bipolar TTL functions. This is because, unlike TTL circuits, CMOS circuits dissipate only negligible power due to leakage currents when they are not switching. The maximum quiescent current per ACL package for SSI (40μA) is less than 1% of that of an equivalent TTL package with 50% of the gates in the High state. The typical dynamic power dissipation of ACL gates is also very low. With 50pF load and a 5V supply, it is 0.18mW at 100kHz rising to only 18mW at 10MHz, two-thirds of which is dissipated in the load capacitance. This is considerably lower than that of the fastest TTL circuits, particularly at lower frequencies where their high quiescent current predominates over their dynamic current.

The power cross-over frequency where ACL and TTL dissipate the same power is about 10MHz for a gate, and more than 20MHz for a flip-flop. However, in a practical logic system, only a few of the logic elements operate at the maximum clock frequency, so the average operating frequency is much lower, giving ACL ICs an even greater advantage over advanced TTL. In a more complex system comprising a divider chain of six flip-flops, the power cross-over frequency no longer exists. At 30MHz, ACL still dissipates only one sixth of the equivalent advanced TTL dissipation. If the divider chain is lengthened, or the system complexity increased, the power saving increases even more.

Propagation Delay

The on-chip propagation for a single ACL gate is only 0.5ns. For an entire ACL package with a 50pF load, it is 5ns average for High-to-Low or Low-to-High transitions. Moreover, propagation delay is specified over the entire operating temperature range and at two system supply voltages (3.3V ± 0.3V and 5V ± 0.5V). For user convenience, we also specify the minimum propagation delay. The specified limits are comparable to those for the most advanced TTL logic. The AC characteristics of ACL are improved by standardized output buffers which allow equal rise and fall times. The typical switching frequency limit for ACL is 150MHz at 25°C and is specified with a 50% duty factor so you don't have to tweak the pulse widths as you do with TTL. Due to the high drive current capability of the low impedance ACL outputs, propagation delay variation as a function of load capacitance is much less than that of most other logic ICs.

Noise Immunity

The input switching levels for 74AC ICs are always between 30% and 70% of V_{CC}. Output swing is from 0.1V to V_{CC} - 0.1V with a load of 50μA (50 CMOS inputs). For 74AC circuits driving 50 CMOS inputs, the low- and high-level noise immunity with a 4.5V supply is, therefor, 28% of V_{CC}. It is even greater for a higher supply voltage, 74ACT ICs match the Low-level noise immunity of TTL at higher operating temperatures (up to 85°C) and exceed it at 70°C. The High-level noise immunity is three times that of TTL. ACL ICs are, therefore, ideally suited for use in electrically noisy environments such as those encountered in industry, telephony and automotive applications.

Drive Capability

Although the ACL family has the low input current which is a characteristic of CMOS circuits, it is capable of providing output current of up to 24mA without sacrifice of noise immunity or switching speed. Moreover, unlike the fastest TTL circuits, all ACL ICs have standardized output buffers which allow symmetrical output current sinking and sourcing to obtain equal rise and fall times. This simplifies design and results in optimum speed and AC performance.

The drive current specified for ACL is valid over the entire operating temperature range and, since the input current for ACL circuits is only 1μA in the High or Low state, the fan-out when driving other CMOS circuits is only limited by load capacitance considerations and not by the available drive power. However, in the fastest logic systems, ACL will probably be working in a transmission line environment where its low output resistance (20Ω max.) is of particular significance for reducing a system's susceptibility to crosstalk and induced noise, and for guaranteeing incident wave switching to optimize system speed. For example, to guarantee incident wave switching over the commercial temperature range, the sink/source capability of ACL is 75mA at V_O=1.65V which allows terminated lines with a characteristic impedance down to 50Ω to be driven at the maximum supply voltage.

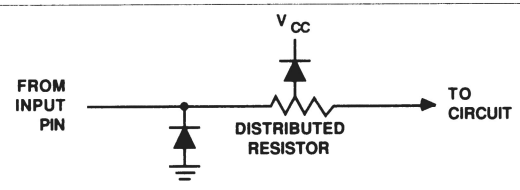
ESD Protection

The ACL input network shown in Figure 2(a) incorporates reverse-biased diodes between the positive rail, input pins and ground in order to clamp the input voltage to provide ESD protection and limit the amplitude of any ringing. These diodes have typical forward voltage drops of 0.9V and reverse breakdown voltages of 18V. ACL inputs can withstand ESD of greater than ±2kV from the 'human body model' (1.5k ohm, 100pF, 13ns pulse rise time) shown in Figure 2(b). This meets MIL-STD-883B, Method 3015.

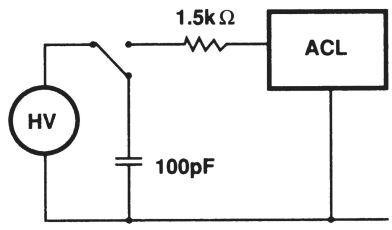
Large inherent diodes formed by the drain surfaces of ACL output transistors provide protection and allow discharges up to 2kV to be sustained without damage to outputs.

ACL is Latch-up Free

Latch-up can be reduced by the use of extensive guard rings, but at the expense of increased chip area. In our ACL family, we've completely eliminated latch-up by growing the high-resistivity p^- epitaxial layer on a very low-resistivity p^+ layer and thereby prevents parasitic bipolar transistors from being forward biased. This, plus proprietary layout rules and process parameters that even further reduce the



(a) ACL Input Protection Network



(b) 'Human Body Model' Test Arrangement

Figure 2. The Inputs of ACL ICs Are Fully Protected Against ESD.

gain of the parasitic bipolar transistors, means that our ACL ICs are completely latch-up free.

We've subjected our ACL ICs to latch-up tests with ratings far exceeding those specified by JEDEC. In no case did latch-up occur. For example, input/outputs can withstand currents as high as 100mA DC or 450mA pulsed. V_{CC} breakdown for ACL ICs doesn't occur until a supply current of 6.8mA; this requires a supply voltage of more than 21V. After breakdown, the supply voltage always snaps back to a level far greater than the maximum operating supply voltage. So, latch-up will not occur in the event of severe supply over voltage.

74ACT - FOR INTERFACING WITH TTL

Since the entire type range of ACL ICs is also available in 74ACT versions, it is easy to drive ACL from ALSTTL, ASTTL or FAST-TTL outputs without using power consuming pull-up resistors at the bipolar logic outputs to maintain adequate noise margins.

All the advantages previously described for 74AC ICs naturally also apply to the 74ACT versions. The only differences are that the propagation delay is slightly longer and the nominal supply voltage and the input structure of the 74ACT types have been modified to match TTL characteristics. The modified input structure not only adapts to TTL input switching levels, but also reduces power consumption when a minimum TTL High output level of 2.4V is applied to a 74ACT input.

For TTL compatibility, the supply voltages for 74ACT ICs is 5V ±10%. Unlike 74AC ICs which have an input switching threshold of 50% of V_{CC}, the input switching threshold of 74ACT types is 1.5V and the inputs switch between the same levels as TTL (V_{ILmax}=0.8V, V_{IHmin}=2V). The temperature sensitivity of the input switching threshold, however, is only ±60mV over the entire temperature range, so the noise margins also remain very stable over the temperature range. With a 4.5V supply and an output current of 50µA (50 ACL inputs), a 74ACT output swings between 0.1V and V_{CC}-0.1V. With the maximum output current of 24mA, it swings between 0.5V and V_{CC}-0.8V. So, for a 74ACT IC with a 4.5V supply driving fifty ACL inputs, the noise margins are 53% of V_{CC} (High) and 15.5% of V_{CC} (Low). For a similar LSTTL IC, they would be only 15% of V_{CC}(High and 8% of V_{CC} (Low). Even when a 74ACT IC is delivering 24mA, the noise margins are 42% of V_{CC} (High) and 6.6% of V_{CC} (Low).

ADVANCED TECHNOLOGY MAKES IT POSSIBLE

The 10-mask ACL construction is a result of our continuing development program to enhance the proven polycrystalline silicon (polysilicon) gate CMOS process. It incorporates several technological innovations for increasing packing density, speed, and reliability.

The twin-well p^-/n^- structure and double-layer metal interconnects allow a high packing density which will also facilitate development of future MSI/LSI circuitry.

Three main features contribute to the exceptionally high speed of ACL. Firstly, the effective length of the transistor gate is only 1µm, resulting in an on-chip propagation delay of only 0.5ns. Secondly, there is a self-aligning titanium disilicide (salicide) layer on the source gate and drain to reduce series resistance and to reduce contact resistance between the 2-layer metal interconnects and the junctions. Thirdly, oxidation of the sidewalls of the gate minimizes the gate/source and gate/drain capacitances.

Reliability is assured by using copper-doped aluminum on tungsten interconnects to achieve high resistance to electromigration. A very thin titanium layer below the tungsten promotes adhesion to

SAFE DRIVING-INTERFACE REQUIREMENTS

Safe driving-interface requirements		TO					
		HC/AC 5V supply	HCT/ACT 5V supply	HE4000B 5V supply	HE4000B 6-15 V supply	TTL* 5V supply	ECL 10K
FROM	HC/AC 5V supply	direct	direct	direct	4104	direct	10124
	HCT/ACT 5V supply	direct	direct	direct	4104	direct	10124
	HE4000B 5V supply	direct	direct	direct	4104	direct	10124
	HE4000B 6-15V supply	4049 or 4050	4049 or 4050	4049 or 4050	direct	4049 or 4050	transistor
	TTL* 5V supply	pull-up resistor	direct	pull-up resistor	4104	direct	10124
	ECL 10K	10125	10125	10125	transistor	10124	direct

* Includes LS, S, STD, FAST, ALS and AS

NOTES:
direct = without interface components
4104 = Low-to-High level shifters from the HE4000B family
10124 = TTL to ECL translator from the ECL 10K and 100K families
10125 = ECL to TTL translator from the ECL 10K and 100K families
4049/4050 = High-to-Low level shifters from the HE4000B family

the underlying oxide. Furthermore, a p^- epitaxial layer on a low-resistivity p^+ substrate results in a high degree of latch-up immunity.

NEW PINOUTS FOR ACL ADD RELIABILITY AND SIMPLIFY DESIGN

The fast rise and fall times associated with high speed logic can lead to noise problems when one or more outputs of an IC switch from one logic state to another. As shown in Figure 3 this discharges the load capacitances through the internal supply pin inductance, thereby causing a transient that lifts up the on-chip ground and reduces the effective supply voltage to the chip. The problems are particularly severe in CMOS logic in which the outputs can switch almost from one supply rail to the other. Referred to as simultaneous switching noise, the transient appears on any unswitched output(s) and has a peak amplitude directly proportional to the number of outputs simultaneously switched and to the internal inductance associated with the IC supply connections. This lifting up of the GND and consequent reduction of V_{CC} levels degrades system reliability by reducing noise margins, reducing speed, causing loss of stored data and causing false switching.

It is a common misconception that supply decoupling capacitors located adjacent to each IC will eliminate simultaneous output switching transients. The output capacitance discharge noise is related to the absolute inductance of the supply connection between the chip in the IC and the external supply groundplane. Since multilayer boards provide excellent supply and groundplanes, improvement can only be achieved by manufacturers taking measures to reduce the supply lead inductances within the IC. Supply line decoupling should be similar to that used for TTL systems operating at comparable speed.

In the early days of integrated logic, IC manufacturers were forced to position the supply pins at diagonally opposite corners of the package because of layout restrictions imposed by single-sided print-boards which were in universal use at that time. However, in today's world of double-sided and multilayer print-boards and much faster logic, placing the supply pins at diagonally opposite corners of the package where the long bonding wires and lead frame segments have the maximum inductance can no longer be considered to be good engineering practice because it's the worst possible positioning from the point of view of simultaneous switching noise. So, for our ACL ICs, we've decided that optimum reliability is far more important than pin compatibility with TTL, and we've relocated the GND and V_{CC} pins; 16-pin ICs with 3 or 4 outputs have two GND pins and two V_{CC} pins; 20, 24 and 28-pin ICs with 3 or more outputs have four GND pins and two V_{CC} pins.

Tests performed on our octal ACL ICs with the new pinning reveal that, when seven outputs are simultaneously switched from High to Low, the amplitude of simultaneous switching noise stays well below the Low input switching level and is only about 35% of that for an IC with corner GND and V_{CC} pins.

We've also rationalized the positioning of the I/O and control pinning of ACL ICs as shown in Figure 4. All the inputs surround the V_{CC} pin(s) on the side of the package with the highest pin numbers, and all the outputs surround the GND pin(s) on the other side of the package. The control pins are strategically placed at the corners of the package. This ACL flow-through architecture, which is used for all ACL ICs in both DIP and SO packages, reduces the total inductance of outputs (bonding wire plus lead frame and output pin) between the chip and the pcb tracks. It also facilitates positioning of decoupling components, simplifies pcb design and fault-finding, and decreases the area of pcb required.

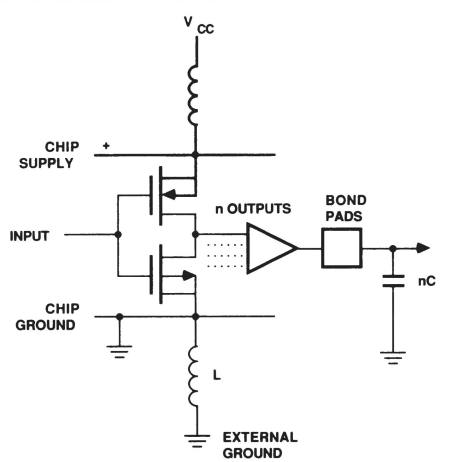


Figure 3

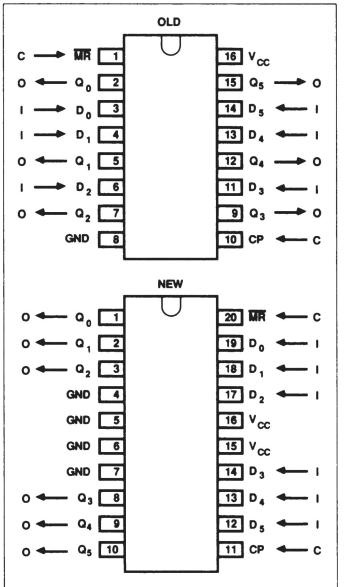


Figure 4. Flow-through Architecture of 74AC11174.

Numeric Index

TYPE NO.	NO. OF PINS	DESCRIPTION	CLASSIFICATION	PAGE
74AC/ACT11000	16	Quad 2-Input NAND Gate	SSI	5-3
74AC/ACT11002	16	Quad 2-Input NOR Gate	SSI	5-7
74AC/ACT11004	20	Hex Inverter	SSI	5-11
74AC/ACT11008	16	Quad 2-Input AND Gate	SSI	5-15
74AC/ACT11010	16	Triple 3-Input NAND Gate	SSI	5-19
74AC/ACT11011	16	Triple 3-Input AND Gate	SSI	5-23
74AC/ACT11013	14	Dual 4-Input NAND Schmitt-Trigger	SSI	5-27
74AC/ACT11014	20	Hex Inverter Schmitt-Trigger	SSI	5-31
74AC/ACT11020	14	Dual 4-Input NAND Gate	SSI	5-35
74AC/ACT11021	14	Dual 4-Input AND Gate	SSI	5-39
74AC/ACT11027	16	Triple 3-Input NOR Gate	SSI	5-43
74AC/ACT11030	14	8-Input NAND Gate	SSI	5-47
74AC/ACT11032	16	Quad 2-Input OR Gate	SSI	5-51
74AC/ACT11034	20	Hex Non-Inverter	SSI	5-55
74AC/ACT11074	14	Dual D-Type Flip-Flop w/Set and Reset; Positive-Edge Trigger	SSI	5-59
74AC/ACT11086	16	Quad 2-Input Exclusive-OR Gate	SSI	5-66
74AC/ACT11109	16	Dual J-K Flip-Flop w/Set and Reset; Positive-Edge Trigger	SSI	5-70
74AC/ACT11112	16	Dual J-K Flip-Flop w/Set and Reset; Negative-Edge Trigger	MSI	5-77
74AC/ACT11132	16	Quad 2-Input NAND Schmitt-Trigger	SSI	5-84
74AC/ACT11138	16	3-to-8 Line Decoder/Demultiplexer; Active-Low	MSI	5-88
74AC/ACT11139	16	Dual 2-to-4 Line Decoder/Demultiplexer; Active-Low	MSI	†
74AC/ACT11151	16	8-Input Multiplexer	MSI	5-94
74AC/ACT11153	16	Dual 4-Input Multiplexer	MSI	†
74AC/ACT11157	20	Quad 2-Input Multiplexer	MS	†
74AC/ACT11158	20	Quad 2-Input Multiplexer, INV	MSI	5-100
74AC/ACT11160	20	Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset	MSI	5-105
74AC/ACT11161	20	Synchronous Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset	MSI	†
74AC/ACT11162	20	Synchronous Presettable Synchronous BCD Decade Counter; Synchronous Reset	MS	5-115
74AC/ACT11163	20	Synchronous Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset	MSI	†
74AC/ACT11168	20	Synchronous Up/Down BCD Decade Counter	MSI	†
74AC/ACT11169	20	Synchronous Presettable 4-Bit Up/Down Binary Decade Counter	MSI	†
74AC/ACT11174	20	Hex D-Type Flip-Flop w/Reset; Positive-Edge Trigger	MSI	†
74AC/ACT11175	20	Quad D-Type Flip-Flop w/Reset; Positive-Edge Trigger	MSI	5-124
74AC/ACT11181	28	4-Bit Arithmetic Logic Unit	MSI	†
74AC/ACT11190	20	Asynchronous Presettable Synchronous Decade Up/Down Counter w/Single Clock	MSI	5-131
74AC/ACT11191	20	Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Single Clock	MS	5-142
74AC/ACT11192	20	Asynchronous Presettable Synchronous BCD Decade Up/Down Counter w/Dual Clock	MSI	†
74AC/ACT11193	20	Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Dual Clock	MSI	†
74AC/ACT11194	20	4-Bit Bidirectional Universal Shift Register	MSI	5-153
74AC/ACT11238	16	3-to-8 Line Decoder/Demultiplexer; Active-High	MSI	5-161
74AC/ACT11239	16	Dual 2-to-4 Line Decoder/Demultiplexer; Active-High	MSI	†
74AC/ACT11240	24	Octal Buffer/Line Driver, INV (3-State)	MSI	5-167
74AC/ACT11241	24	Octal Buffer/Line Driver (3-State)	MS	5-171
74AC/ACT11244	24	Octal Buffer/Line Driver (3-State)	MSI	5-175
74AC/ACT11245	24	Octal Transceiver w/Direction Pin (3-State)	MSI	5-179
74AC/ACT11251	16	8-Input Multiplexer (3-State)	MSI	5-183
74AC/ACT11253	16	Dual 4-Input Multiplexer (3-State)	MS	5-189
74AC/ACT11257	20	Quad 2-Input Multiplexer (3-State)	MSI	5-195
74AC/ACT11258	20	Quad 2-Input Multiplexer, INV (3-State)	MSI	5-201
74AC/ACT11269	28	Synchronous Presettable 8-Bit Binary Up/Down Counter	MSI	†
74AC/ACT11280	14	9-Bit Odd/Even Parity Generator/Checker	MSI	5-207
74AC/ACT11286	14	9-Bit Odd/Even Parity Generator/Checker w/Bus Drive I/O Port	MSI	5-212
74AC/ACT11299	24	8-Input Universal Shift/Storage Register w/Asynchronous Reset and Common I/O Pins	MSI	†
74AC/ACT11323	24	8-Input Universal Shift/Storage Register w/Synchronous Reset and Common I/O Pins	MSI	†
74AC/ACT11352	16	Dual 4-Input Multiplexer, INV	MSI	†

† For more information on these devices contact your local sales organization; see addresses on back cover.

TYPE NO.	NO. OF PINS	DESCRIPTION	CLASSIFICATION	PAGE
74AC/ACT11353	16	Dual 4-Input Multiplexer, INV (3-State)	MSI	5-218
74AC/ACT11373	24	Octal D-Type Transparent Latch (3-State)	MS	5-224
74AC/ACT11374	24	Octal D-Type Flip-Flop; Positive-Edge Trigger: 3-State	MSI	5-231
74AC/ACT11378	20	Hex D-Type Flip-Flop w/Enable; Positive-Edge Trigger	MSI	†
74AC/ACT11379	20	Quad D-Type Flip-Flop w/Data Enable	MSI	†
74AC/ACT11520	20	8-Bit Identity Comparator w/Input Pull-Up	MS	5-237
74AC/ACT11521	20	8-Bit Identity Comparator	MSI	5-242
74AC/ACT11533	24	Octal D-Type Transparent Latch, INV (3-State)	MSI	5-247
74AC/ACT11534	24	Octal D-Type Flip-Flop; Positive-Edge Trigger, INV (3-State)	MS	5-254
74AC/ACT11568	24	Synch. Presettable BCD Decade Up/Down Counter w/Synch. and Asynch. Reset	MS	†
74AC/ACT11569	24	Synch. Presettable 4-Bit Binary Up/Down Counter w/Synch. and Asynch. Reset	MSI	†
74AC/ACT11579	24	8-Bit Binary Up/Down Counter w/Common I/O Pins; Synch. and Asynch. Reset (3-State)	MSI	†
74AC/ACT11620	24	Octal Transceiver w/Dual Enable: 3-State, INV	MS	†
74AC/ACT11623	24	Octal Transceiver w/Dual Enable (3-State)	MSI	†
74AC/ACT11640	24	Octal Transceiver w/Direction Pin, INV (3-State)	MSI	5-260
74AC/ACT11643	24	Octal Transceiver (3-State); True/INV	MSI	†
74AC/ACT11646	28	Octal Transceiver/Register w/Direction Pin (3-State)	MSI	†
74AC/ACT11648	28	Octal Transceiver/Register w/Direction Pin, INV (3-State)	MSI	†
74AC/ACT11651	28	Octal Transceiver/Register w/Dual Enable, INV (3-State)	MSI	†
74AC/ACT11652	28	Octal Transceiver/Register w/Dual Enable (3-State)	MSI	†
74AC/ACT11657	28	Octal Transceiver w/8-Bit Parity Checker/Generator	MSI	†
74AC/ACT11810	16	Quad 2-Input Exclusive-NOR Gate	SSI	5-264
74AC/ACT11818	28	8-Bit Diagnostic/Pipe-Line Register	MSI	†
74AC/ACT11819	28	8-Bit Diagnostic/Pipe-Line Register w/Parity Even Output	MS	†
74AC/ACT11821	28	10-Wide D-Type Flip-Flop; Positive-Edge Trigger (3-State)	MSI	†
74AC/ACT11822	28	10-Wide D-Type Flip-Flop; Positive-Edge Trigger (3-State): , INV	MSI	†
74AC/ACT11823	28	9-Wide D-Type Flip-Flop w/Reset and Enable; Positive-Edge Trigger (3-State)	MSI	†
74AC/ACT11824	28	9-Wide D-Type Flip-Flip w/Reset and Enable; Positive-Edge Trigger, INV (3-State)	MS	†
74AC/ACT11825	28	Octal D-Type Flip-Flop w/Reset and Enable; Positive-Edge Trigger (3-State)	MSI	†
74AC/ACT11826	28	Octal D-Type Flip-Flop w/Reset and Enable; Positive-Edge Trigger, INV (3-State)	MS	†
74AC/ACT11827	28	10-Wide Buffer/Line Driver (3-State)	MSI	†
74AC/ACT11828	28	10-Wide Buffer/Line Driver, INV (3-State)	MSI	†
74AC/ACT11833	28	8-Bit Transceiver w/9-Bit Parity Checker/Generator and Error Flip-Flop	MSI	†
74AC/ACT11834	28	8-Bit, INV Transceiver w/9-Bit Parity Checker/Generator and Error Flip-Flop	MSI	†
74AC/ACT11841	28	10-Wide D-Type Transparent Latch (3-State)	MSI	†
74AC/ACT11842	28	10-Wide D-Type Transparent Latch, INV (3-State)	MSI	†
74AC/ACT11843	28	9-Wide D-Type Transparent Latch w/Set and Reset (3-State)	MSI	†
74AC/ACT11844	28	9-Wide D-Type Transparent Latch w/Set and Reset, INV (3-State)	MSI	†
74AC/ACT11845	28	Octal D-Type Transparent Latch w/Set and Reset (3-State)	MSI	†
74AC/ACT11846	28	Octal D-Type Transparent Latch w/Set and Reset, INV (3-State)	MSI	†
74AC/ACT11853	28	8-Bit Transceiver w/9-Bit Parity Checker/Generator and Error Flag Latch	MSI	†
74AC/ACT11854	**28**	**8-Bit INV Transceiver with 9-Bit Parity Checker/Generator and Error Flag Latch**	**MSI**	†
74AC/ACT11861	28	10-Wide Transceiver (3-State)	MSI	†
74AC/ACT11862	28	10-Wide Transceiver (3-State): , INV	MS	†
74AC/ACT11863	28	9-Wide Transceiver: 3-State	MSI	†
74AC/ACT11864	28	9-Wide Transceiver, INV (3-State)	MSI	†
74AC/ACT11873	28	Dual D-Type 4-Bit Transparent Latch w/Reset (3-State)	MSI	†
74AC/ACT11874	28	Dual D-Type 4-Bit Flip-Flop Latch w/Reset (3-State)	MSI	†
74AC/ACT11881	28	4-Bit Arithmetic Logic Unit w/Status Check Register	MSI	†
74AC/ACT11882	28	32-Bit Look-Ahead Carry Generator	MS	†
74AC/ACT11898	20	10-Bit Serial-In Parallel-Out Shift Register	MSI	5-268

† For more information on these devices contact your local sales organization; see addresses on back cover.

Functional Index

ACL 74AC/ACT11XXX FAMILY

Type numbers have a suffix which signifies the type of package:
N = Plastic DIP; D = Plastic Surface Mount Device

TYPE NO.	NO. OF PINS	DESCRIPTION	CLASSIFICATION	PAGE
NAND/NOR Gates				
74AC/ACT11000	16	Quad 2-Input NAND Gate	SSI	5-3
74AC/ACT11002	16	Quad 2-Input NOR Gate	SSI	5-7
74AC/ACT11010	16	Triple 3-Input NAND Gate	SSI	5-19
74AC/ACT11013	14	Dual 4-Input NAND Schmitt Trigger	SSI	5-27
74AC/ACT11020	14	Dual 4-Input NAND Gate	SSI	5-35
74AC/ACT11027	16	Triple 3-Input NOR Gate	SSI	5-43
74AC/ACT11030	14	8-Input NAND Gate	SSI	5-47
74AC/ACT11132	16	Quad 2-Input NAND Schmitt Trigger	SSI	5-84
AND/OR Gates				
74AC/ACT11008	16	Quad 2-Input AND Gate	SSI	5-15
74AC/ACT11011	16	Triple 3-Input AND Gate	SSI	5-23
74AC/ACT11021	14	Dual 4-Input AND Gate	SSI	5-39
74AC/ACT11032	16	Quad 2-Input OR Gate	SSI	5-51
74AC/ACT11086	16	Quad 2-Input Exclusive-OR Gate	SSI	5-66
74AC/ACT11810	16	Quad 2-Input Exclusive-NOR Gate	SSI	5-264
Inverters/Buffers/Line Drivers				
74AC/ACT11004	20	Hex Inverter	SSI	5-11
74AC/ACT11014	20	Hex Inverter Schmitt Trigger	SSI	5-31
74AC/ACT11034	20	Hex Non-Inverter	SSI	5-55
74AC/ACT11240	24	Octal Buffer/Line Driver, INV (3-State)	MSI	5-167
74AC/ACT11241	24	Octal Buffer/Line Driver (3-State)	MSI	5-171
74AC/ACT11244	24	Octal Buffer/Line Driver (3-State)	MSI	5-175
74AC/ACT11827	28	10-Wide Buffer/Line Driver (3-State)	MSI	†
74AC/ACT11828	28	10-Wide Buffer/Line Driver, INV (3-State)	MSI	†

† For more information on these devices contact your local sales organization; see addresses on back cover.

ACL 74AC/ACT11XXX FAMILY

Type numbers have a suffix which signifies the type of package:
N = Plastic DIP; D = Plastic Surface Mount Device

TYPE NO.	NO. OF PINS	DESCRIPTION	CLASSIFICATION	PAGE
Flip-Flops/Latches				
74AC/ACT11074	14	Dual D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger	SSI	5-59
74AC/ACT11109	16	Dual J-K Flip-Flop with Set and Reset; Positive-Edge Trigger	SSI	5-70
74AC/ACT11112	16	Dual J-K Flip-Flop with Set and Reset; Negative-Edge Trigger	MSI	5-77
74AC/ACT11174	20	Hex D-Type Flip-Flop with Reset; Positive-Edge Trigger	MSI	†
74AC/ACT11175	20	Quad D-Type Flip-Flop with Reset; Positive-Edge Trigger	MSI	5-124
74AC/ACT11373	24	Octal D-Type Transparent Latch (3-State)	MSI	5-224
74AC/ACT11374	24	Octal D-Type Flip-Flop; Positive-Edge Trigger (3-State)	MSI	5-231
74AC/ACT11378	20	Hex D-Type Flip-Flop with Enable; Positive-Edge Trigger	MSI	†
74AC/ACT11379	20	Quad D-Type Flip-Flop with Data Enable	MSI	†
74AC/ACT11533	24	Octal D-Type Transparent Latch, INV (3-State)	MSI	5-247
74AC/ACT11534	24	Octal D-Type Flip-Flop; Positive-Edge Trigger, INV (3-State)	MSI	5-254
74AC/ACT11821	28	10-Wide D-Type Flip-Flop; Positive-Edge Trigger (3-State)	MSI	†
74AC/ACT11822	28	10-Wide D-Type Flip-Flop; Positive-Edge Trigger, INV (3-State)	MSI	†
74AC/ACT11823	28	9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger (3-State)	MSI	†
74AC/ACT11824	28	9-Wide D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger, INV (3-State)	MSI	†
74AC/ACT11825	28	Octal D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger (3-State)	MSI	†
74AC/ACT11826	28	Octal D-Type Flip-Flop with Reset and Enable; Positive-Edge Trigger, INV (3-State)	MSI	†
74AC/ACT11841	28	10-Wide D-Type Transparent Latch (3-State)	MSI	†
74AC/ACT11842	28	10-Wide D-Type Transparent Latch, INV (3-State)	MSI	†
74AC/ACT11843	28	9-Wide D-Type Transparent Latch with Set and Reset (3-State)	MSI	†
74AC/ACT11844	28	9-Wide D-Type Transparent Latch with Set and Reset, INV (3-State)	MSI	†
74AC/ACT11845	28	Octal D-Type Transparent Latch with Set and Reset (3-State)	MSI	†
74AC/ACT11846	28	Octal D-Type Transparent Latch with Set and Reset, INV (3-State)	MSI	†
74AC/ACT11873	28	Dual D-Type 4-Bit Transparent Latch with Reset (3-State)	MSI	†
74AC/ACT11874	28	Dual D-Type 4-Bit Flip-Flop Latch with Reset (3-State)	MSI	†
Registers				
74AC/ACT11194	20	4-Bit Bidirectional Universal Shift Register	MSI	5-153
74AC/ACT11299	24	8-Input Universal Shift/Storage Register with Asynchronous Reset and Common I/O Pins	MSI	†
74AC/ACT11323	24	8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins	MSI	†
74AC/ACT11818	28	8-Bit Diagnostic/Pipe-Line Register	MSI	†
74AC/ACT11819	28	8-Bit Diagnostic/Pipe-Line Register with Parity Even Output	MSI	†
74AC/ACT11898	20	10-Bit Serial-In Parallel-Out Shift Register	MSI	5-268
Arithmetic Circuits				
74AC/ACT11181	28	4-Bit Arithmetic Logic Unit	MSI	†
74AC/ACT11280	14	9-Bit Odd/Even Parity Generator/Checker	MSI	5-207
74AC/ACT11286	14	9-Bit Odd/Even Parity Generator/Checker with Bus Drive I/O Port	MSI	5-212
74AC/ACT11520	20	8-Bit Identity Comparator with Input Pull-Up	MSI	5-237
74AC/ACT11521	20	8-Bit Identity Comparator	MSI	5-242
74AC/ACT11881	28	4-Bit Arithmetic Logic Unit with Status Check Register	MSI	†
74AC/ACT11882	28	32-Bit Look-Ahead Carry Generator	MSI	†

† For more information on these devices contact your local sales organization; see addresses on back cover.

ACL 74AC/ACT11XXX FAMILY

Type numbers have a suffix which signifies the type of package:
N = Plastic DIP; D = Plastic Surface Mount Device

TYPE NO.	NO. OF PINS	DESCRIPTION	CLASSIFICATION	PAGE
Counters				
74AC/ACT11160	20	Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset	MSI	5-105
74AC/ACT11161	20	Synchronous Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset	MSI	†
74AC/ACT11162	20	Synchronous Presettable Synchronous BCD Decade Counter; Synchronous Reset	MSI	5-115
74AC/ACT11163	20	Synchronous Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset	MSI	†
74AC/ACT11168	20	Synchronous Up/Down BCD Decade Counter	MSI	†
74AC/ACT11169	20	Synchronous Presettable 4-Bit Up/Down Binary Decade Counter	MSI	†
74AC/ACT11190	20	Asynchronous Presettable Synchronous Decade Up/Down Counter with Single Clock	MSI	5-131
74AC/ACT11191	20	Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter with Single Clock	MSI	5-142
74AC/ACT11192	20	Asynchronous Presettable Synchronous BCD Decade Up/Down Counter with Dual Clock	MSI	†
74AC/ACT11193	20	Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter with Dual Clock	MSI	†
74AC/ACT11269	28	Synchronous Presettable 8-Bit Binary Up/Down Counter	MSI	†
74AC/ACT11568	24	Sync. Presettable BCD Decade Up/Down Counter with Synch. and Asynch. Reset	MSI	†
74AC/ACT11569	24	Synch. Presettable 4-Bit Binary Up/Down Counter with Synch. and Asynch. Reset	MSI	†
74AC/ACT11579	24	8-Bit Binary Up/Down Counter with Common I/O Pins; Synch. and Asynch. Reset (3-State)	MSI	†
Multiplexers				
74AC/ACT11151	16	8-Input Multiplexer	MSI	5-94
74AC/ACT11153	16	Dual 4-Input Multiplexer	MSI	†
74AC/ACT11157	20	Quad 2-Input Multiplexer	MSI	†
74AC/ACT11158	20	Quad 2-Input Multiplexer, INV	MSI	5-100
74AC/ACT11251	16	8-Input Multiplexer (3-State)	MSI	5-183
74AC/ACT11253	16	Dual 4-Input Multiplexer (3-State)	MSI	5-189
74AC/ACT11257	20	Quad 2-Input Multiplexer (3-State)	MSI	5-195
74AC/ACT11258	20	Quad 2-Input Multiplexer, INV (3-State)	MSI	5-201
74AC/ACT11352	16	Dual 4-Input Multiplexer, INV	MSI	†
74AC/ACT11353	16	Dual 4-Input Multiplexer, INV (3-State)	MSI	5-218
Decoder/Demultiplexers				
74AC/ACT11138	16	3-to=8 Line Decoder/Demultiplexer; Active-Low	MSI	5-88
74AC/ACT11139	16	Dual 2-to-4 Line Decoder/Demultiplexer; Active-Low	MSI	†
74AC/ACT11238	16	3-to-8 Line Decoder/Demultiplexer; Active-High	MSI	5-161
74AC/ACT11239	16	Dual 2-to-4 Line Decoder/Demultiplexer; Active-High	MSI	†
Transceivers				
74AC/ACT11245	24	Octal Transceiver with Direction Pin (3-State)	MSI	5-109
74AC/ACT11620	24	Octal Transceiver with Dual Enable, INV (3-State)	MSI	†
74AC/ACT11623	24	Octal Transceiver with Dual Enable (3-State)	MSI	†
74AC/ACT11640	24	Octal Transceiver with Direction Pin, INV (3-State)	MSI	5-260
74AC/ACT11643	24	Octal Transceiver (3-State); True/INV	MSI	†
74AC/ACT11646	28	Octal Transceiver/Register with Direction Pin (3-State)	MSI	†
74AC/ACT11648	28	Octal Transceiver/Register with Direction Pin, INV (3-State)	MSI	†
74AC/ACT11651	28	Octal Transceiver/Register with Dual Enable, INV (3-State)	MSI	†
74AC/ACT11652	28	Octal Transceiver/Register with Dual Enable (3-State)	MSI	†
74AC/ACT11657	28	Octal Transceiver with 8-Bit Parity Checker/Generator	MSI	†
74AC/ACT11833	28	8-Bit Transceiver with 9-Bit Parity Checker/Generator and Error Flip-Flop	MSI	†
74AC/ACT11834	28	8-Bit INV Transceiver with 9-Bit Parity Checker/Generator and Error Flip-Flop	MSI	†
74AC/ACT11853	28	8-Bit Transceiver with 9-Bit Parity Checker/Generator and Error Flag Latch	MSI	†
74AC/ACT11854	28	8-Bit INV Transceiver with 9-Bit Parity Checker/Generator and Error Flag Latch	MSI	†
74AC/ACT11861	28	10-Wide Transceiver (3-State)	MSI	†
74AC/ACT11862	28	10-Wide Transceiver, INV (3-State)	MSI	†
74AC/ACT11863	28	9-Wide Transceiver (3-State)	MSI	†
74AC/ACT11864	28	9-Wide Transceiver, INV (3-State)	MSI	†

† For more information on these devices contact your local sales organization; see addresses on back cover.

ACL 74AC/ACT11XXX FAMILY

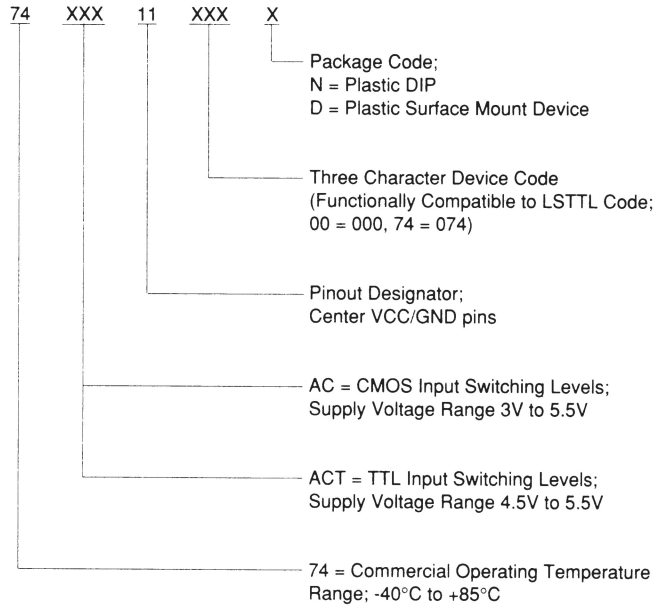
Type numbers have a suffix which signifies the type of package:
N = Plastic DIP; D = Plastic Surface Mount Device

TYPE NO.	NO. OF PINS	DESCRIPTION	CLASSIFICATION	PAGE
Schmitt-Triggers				
74AC/ACT11013	14	Dual 4-Input NAND Schmitt-Trigger	SSI	5-27
74AC/ACT11014	20	Hex Inverter Schmitt Trigger	SSI	5-31
74AC/ACT11132	16	Quad 2-Input NAND Schmitt Trigger	SSI	5-84

† For more information on these devices contact your local sales organization; see addresses on back cover.

Ordering Information

TYPE NUMBER DESIGNATIONS


74 XXX 11 XXX X
Package Code;
N = Plastic DIP
D = Plastic Surface Mount Device
Three Character Device Code
(Functionally Compatible to LSTTL Code;
00 = 000, 74 = 074)
Pinout Designator;
Center VCC/GND pins
AC = CMOS Input Switching Levels;
Supply Voltage Range 3V to 5.5V
ACT = TTL Input Switching Levels;
Supply Voltage Range 4.5V to 5.5V
74 = Commercial Operating Temperature
Range; -40°C to +85°C

Section 2
Quality And Reliability

Quality And Reliability

SIGNETICS LOGIC PRODUCTS QUALITY

Signetics has put together a winning process for manufacturing Logic Products. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The products produced in the Standard Products Division must meet rigid criteria as defined by our design rules and evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic And Uniform Reliability Evaluation) Program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 A/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to ensure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from −55°C to +125°C and at ±10% supply voltage.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes, and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 – QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic And Uniform Reliability Evaluation) Program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE Program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of Logic products, samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: T_J = 150°C, 1000 hours, static biased or dynamic operation, as appropriate (worst case bias configuration is chosen)
- High Temperature Storage: T_J = 150°C, 1000 hours
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static biased
- Temperature Cycling (Air-to-Air): −65°C to +150°C, 1000 cycles

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15psig, 121°C, 100% saturated steam) and 300 cycles of thermal shock (−65°C to +150°C)

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms, and an estimated failure rate resulting from each stress. This data is published quarterly and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the corporate SURE Program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

The engineering process includes:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional, and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, and, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits derived from quality products can best be summed up in the words, *lower cost of ownership.*

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times, and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100PPM (parts per million), down from an industry practice of 10,000PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees; from the R and D laboratory to the shipping dock. In short, we needed a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Signetics' high quality levels have allowed us a "ship-to-stock" program where many major customers no longer need to perform incoming inspection. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers have reported a significant improvement in overall quality (see Figure 1).

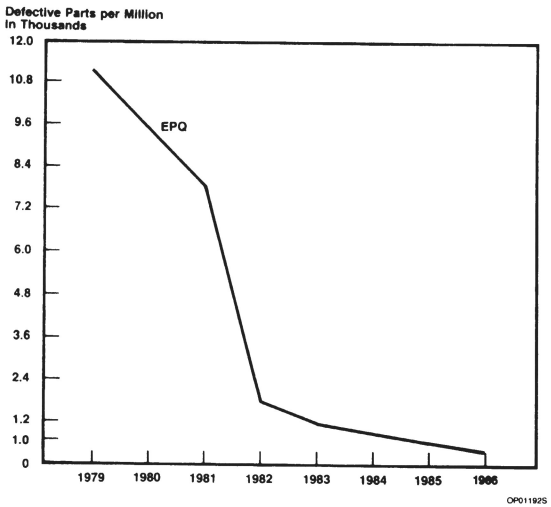


Figure 1. Signetics Quality Progress

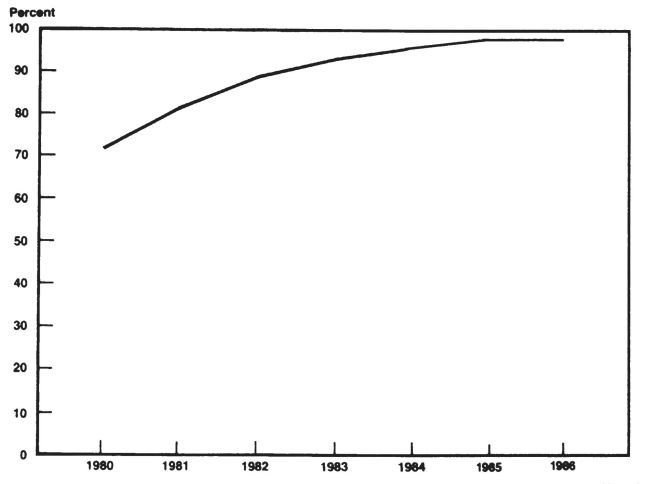


Figure 2. Performance To Schedule On-Time Delivery

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed upon price (see Figure 2).

ONGOING QUALITY PROGRAM

The Quality Improvement Program at Signetics is based on "Do it Right the First Time". The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared equally by all technical and administrative functions.

This program extends into every area of the company and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" – ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" Program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent.

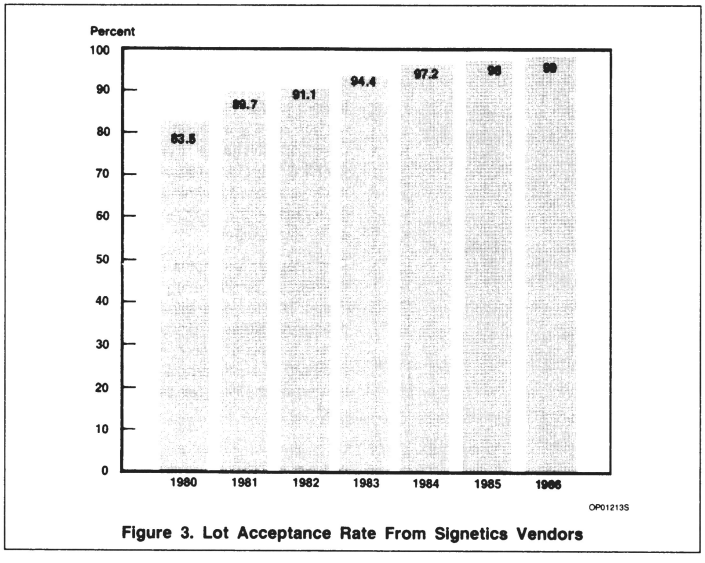


Figure 3. Lot Acceptance Rate From Signetics Vendors

Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

MATERIAL WAIVERS

1986 – 0
1985 – 0
1984 – 0
1983 – 0
1982 – 2
1981 – 134

Higher incoming quality material ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities – failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers. Or, write on your letter-head directly to the corporate director of quality at the corporate address shown at the back of this manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

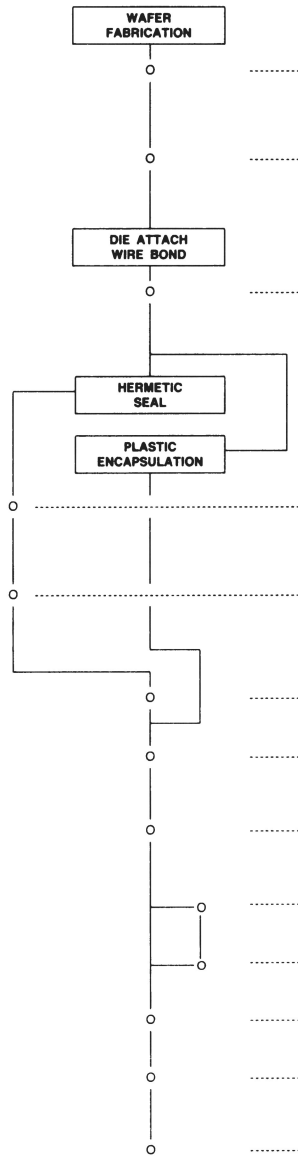
- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This team work with you will allow us to achieve our mutual goal of improved product quality.

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the Quality Improvement Program. During the development of the program many profound changes were made. Figure 4, *Logic Products Generic Process Flow*, shows the result. Some of the other changes and additions were to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading Quality supplier of Logic products. These achievements have also led to our participation in several Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

STABILIZATION BAKE PRECONDITIONING

Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance. Hermetic devices are baked to ensure the elimination of any remaining cavity moisture.

TEMPERATURE CYCLING

Using MIL-STD-883 Method 1010.1 Condition C devices are cycled from cold to hot temperatures imposing a very severe stress which weakens loose bonds and package seals without degrading good devices. A loosened bond is later detected during 100% electrical tests.

SEAL TESTS

Hermetic package seal integrity is ensured by 100% gross leak testing.

SYMBOL

Devices are marked with the Signetics Logo, device number, and date code or custom symbol per individual specification requirements.

100% ELECTRICAL TEST

Every device is tested for functional and AC/DC parameters at room temperature with guard bands to assure performance to data sheet limits.

BURN-IN (SUPR II LEVEL B OPTION)

Devices are burned-in for 21 hours at 155°C junction temperature.

POST-BURN-IN ELECTRICAL TEST

Test to the same stringent test programs and conditions as those used at the pre-burn-in.

VISUAL

All products are 100% visually inspected per the requirements specified in Signetics or customer documents.

PRODUCT ASSURANCE TESTING

Each lot is sampled and tested for functional and DC at 0°C and + 70°C, and AC/DC and functional at 25°C to assure device performance to data sheet limits.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step guarantees that the specified mechanical and electrical requirements have been met. Every shipment is sealed with the craftsman's stamp.

NOTE: The items on this flowchart do not all happen in the same sequence for all products.

Figure 4. Logic Products Generic Process Flow

QUALITY AND RELIABILITY

As time goes on, the drive for ZERO DEFECTS will grow in intensity. As we approach this goal, new measurement tools are required. Statistical Process Control (SPC) will be the approach Signetics uses to further our drive towards ZERO DEFECTS. These efforts will provide both Signetics and their customers with the ability to achieve the mutual goal of improved product quality.

SPC

Application of statistics activities goes back to the early 1970s. Corporate-wide emphasis, however, did not come about until mid-1984. Emphasis was then shifted from a sporadic and uncoordinated effort to a coordinated and disciplined approach. This shift in emphasis came about for two primary reasons:

1. Customers' realization of importance and relevance of SPC to quality and reliability issues; and
2. A natural evolution of our quality process made introduction of SPC and other related programs an inevitable event.

Objective

The objective of the SPC Program is to introduce a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information, and make decisions solely based on data.

Organization

The Vice President of Quality and Reliability with the Corporate SPC Steering Committee set directions for the company. Each operating area has a dedicated SPC Coordinator. Some areas have dedicated statisticians.

In each operating area, QITs are responsible for quality process implementation. SPC coordinators are responsible to these teams tc provide the focus needed for training and implementation.

Training

A two-day course on Crosby's 14-Step improvement program, and a one-day course on basic problem solving techniques are prerequisites to the formal SPC I (Introduction to SPC) training. The intent of SPC I is to bridge the subtle differences between Crosby's and Deming's approach to quality, emphasizing increased application of statistical methodology.

Signetics' philosophy is to do **just-in-time** training rather than **just-in-case** training. Senior management, middle management, supervisors, and operators are required to take the training courses offered in SPC. As the application of SPC evolves, training will be provided by previously trained coordinators/supervisors who will be instructed to identify and remove sources of excessive variation within their departments/areas, and to develop and maintain a permanent control system.

Conclusion

The most critical and challenging aspect of implementing SPC is establishment of a discipline within the operating areas where decision making is fundamentally based on verifiable data, and actions are clearly documented. The other is realization of the fact that statistical tools merely point out the problems and are **not** solutions by themselves.

In order to implement SPC effectively, three steps must be continually used:

1. Document and understand the process, using process flow charts and component diagrams.
2. Establish data collection systems and use SPC tools to identify process problems and opportunities for improvement.
3. Act on the process, establish guidelines to monitor and maintain process control.

Because of the nature of the SPC process, steps 1, 2, and 3 are repeated again and again. By doing this, the department/area begins to modify its day-to-day activities, making job functions and procedures more efficient and effective.

The real measure of any quality improvement program is the result that the customer sees. The meaning of **Quality** is more than just working circuits. It means commitment to **On-Time Delivery** to the **Right Place,** of the **Right Quantity,** of the **Right Product,** at the **Agreed Upon Price.**

Section 3
Family Characteristics

INDEX

Family Specifications 3-3
Data Sheet Specification Guide 3-6
Definitions and Symbols 3-8

Family Specifications

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire 74AC/ACT11XXX family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74AC/ACT11XXX 1μm CMOS Logic family combines the low power advantages of CMOS with the high speed and drive capability of FAST.

The basic family of devices designated as 74AC11XXX will operate at CMOS input logic levels for high noise immunity, negligible quiescent supply and input current. It is operated from a power supply of 3 to 5.5V.

A subset of the family designated as 74ACT11XXX with the same features and functions as the "AC-types" will operate at standard TTL power supply voltage (5V±10%) and logic input levels (0.8 to 2.0V).

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

However, to be totally safe, it is desirable to take handling precautions into account (also see AN600 "Handling Precautions" in Section 5).

SOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current	n = number of outputs (but not less than 100mA)	±(n × 25)	mA
	DC ground current	n = number of outputs (but not less than 100mA)	±(n × 25)	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11000				74ACT11000				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OH} = 12mA	3.0		0.36		0.44					
			I_{OH} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OH} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	µA
I_{CC}	Quiescent supply current, for SSI	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	µA
	Quiescent supply current, for MSI	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11000			74ACT11000			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

Data Sheet Specification Guide

INTRODUCTION

The 74ACL data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of t_{PLH} and t_{PHL} for a typical data path through the device with a 50pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on t_R and t_F.

LOGIC SYMBOLS

Two logic symbols are given for each device - the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEEE/IEC Logic Symbol.

The IEEE/IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table lists the maximum limits to which the device can be subjected without damage. This does not imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life will not have been shortened.

RECOMMENDED OPERATING CONDITIONS

The "Recommended Operating Conditions" table lists the operating ambient temperature and the conditions under which the limits in the "DC Characteristics" and "AC Characteristics" table will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC Characteristics tables.

TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground plate) should be used for the same reasons. A V_{CC} decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 3ns, a signal swing of 0V to V_{CC} for 74AC and 0V to 3V for 74ACT; a 5MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters as setup time, hold time and removal time. f_{MAX} is also tested with 3ns input rise and fall times, with a 50% duty factor, but for typical f_{MAX} as high as 150MHz, there are no constraints on rise and fall times.

DC CHARACTERISTICS

The "DC Characteristics" table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of V_{IH} and V_{IL} are applied to the inputs, the output voltages will be those published in the "DC Characteristics" table. There is a tendency, by some, to use the published V_{IH} and V_{IL} thresholds to test a device for functionality in a "function-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 meter. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use V_{IH} and V_{IL} to test the functionality of any ACL device type; instead, use input voltages of V_{CC} (for the High state) and 0V (for the Low state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical V_{IL} is higher than the maximum V_{IL}. However, this is because $V_{IL\,MAX}$ is the maximum V_{IL} (guaranteed) for all devices that will be recognized as a logic Low. However, typically a higher V_{IL} will also be recognized as a logic Low. Conversely, the typical V_{IH} is lower than its minimum guaranteed level.

The quiescent supply current I_{CC} is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors.

AC CHARACTERISTICS

The "AC Characteristics" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveform section.

Definitions of Symbols

DEFINITIONS OF SYMBOLS AND TERMS USED IN ACL DATA SHEETS

Current

Positive current is defined as conventional current flow into a device.

Negative current is defined as conventional current flow out of a device.

I_{cc} Quiescent power supply current; the current flowing into the V_{CC} supply terminal.

ΔI_{cc} Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.

I_{GND} Quiescent power supply current; the current flowing into the GND terminal.

I_I Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} Input diode current; the current flowing into a device at a specified input voltage.

I_O Output source or sink current; the current flowing into a device at a specified output voltage.

I_{OK} Output diode current; the current flowing into a device at a specified output voltage.

I_{OZ} OFF-state output current; the leakage current flowing into the output of a 3-State device in the OFF-state, when the output is connected to V_{CC} or GND.

Voltages

All voltages are referenced to GND (ground), which is typically 0V.

GND Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power supplies.

V_H Hysteresis voltage; difference between the trigger levels when applying a positive and a negative-going input signal.

V_{IH} High-level input voltage; the range of input voltages that represents a logic High-level in the system.

V_{IL} Low-level input voltage; the range of input voltages that represents a logic Low-level in the system.

V_{OH} High-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a High-level at the output.

V_{OL} Low-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a Low-level at the output.

V_{T+} Trigger threshold voltage; positive-going signal.

V_{T-} Trigger threshold voltage; negative-going signal.

Capacitances

C_I Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$ Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PD} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function when no extra load is provided to the device.

AC Switching Parameters

f_I Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate High and Low for data input or using the toggle mode, whichever is applicable.

f_O Output frequency; each output.

f_{MAX} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10% V_{CC} to 90% V_{CC} in accordance with device function table.

t_H Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_R, t_F Clock input rise and fall times; 10% and 90% values.

t_{PHL} Propagation delay; the time between the specified reference points, normally the 50% points for 74AC devices on the input and output waveforms and the 1.5V points for the 74ACT devices, with the output changing from the defined High-level to the defined Low-level.

t_{PLH} Propagation delay; the time between the specified reference points, normally the 50% points for 74AC devices on the input and output waveforms and the 1.5V point for the 74ACT devices, with the output changing from the defined Low-level to the defined High-level.

t_{PHZ} 3-State output disable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and a point representing 20% of the output swing on the output voltage waveform of a 3-State device, with the output changing from a High-level (V_{OH}) to a high-impedance OFF-state (Z).

t_{PLZ} 3-State output disable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and a point representing 20% of the output swing on the output voltage waveform of a 3-State device, with the output changing from a Low-level (V_{OL}) to a high-impedance OFF-state (Z).

t_{PZH} 3-State output enable time; the time between the specified reference points, normally the 50% points for the 74AC devices and 1.5V points for the 74ACT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-State device, with the output changing from a high-impedance OFF-state (Z) to a High-level (V_{OH}).

t_{PZL} 3-State output enable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-State device with the output changing from a high-impedance OFF-state (Z) to a Low-level (V_{OL}).

t_{REM} Removal time; the time between the end of and overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for 74AC devices and the 1.5V points for the 74ACT devices on both input voltage waveforms.

t_S Setup time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval data to be recognized must be maintained at the input to ensure their recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High-to-Low.

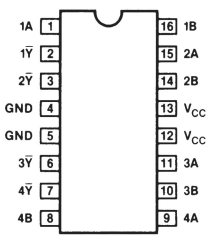
t_{TLH} Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low-to-High.

t_W Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for 74AC devices and at the 1.5V points for 74ACT devices.

Section 4
ACL Pinouts

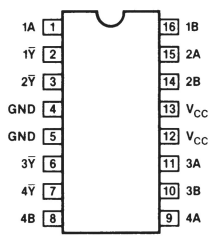
ACL Pinouts

11000



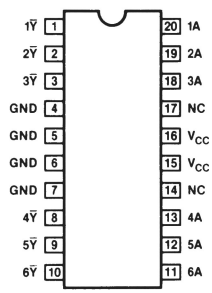
Quad 2-Input NAND Gate

11002



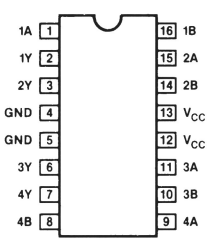
Quad 2-Input NOR Gate

11004



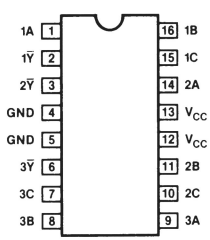
Hex Inverter

11008



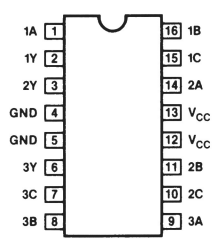
Quad 2-Input AND Gate

11010



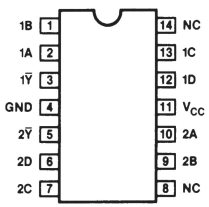
Triple 3-Input NAND Gate

11011



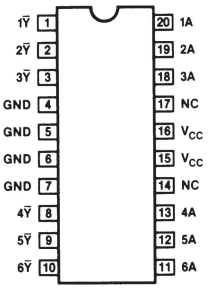
Triple 3-Input AND Gate

11013



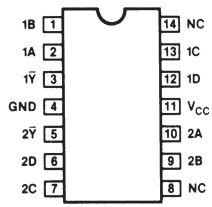
Dual 4-Input NAND Schmitt-Trigger

11014



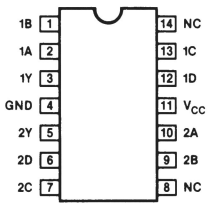
Hex Inverter Schmitt-Trigger

11020



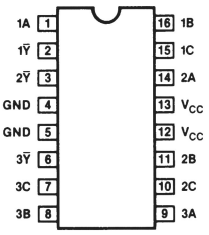
Dual 4-Input NAND Gate

11021



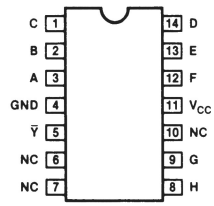
Dual 4-Input AND Gate

11027



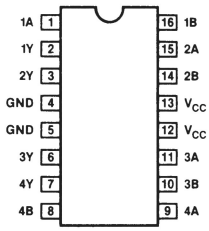
Triple 3-Input NOR Gate

11030



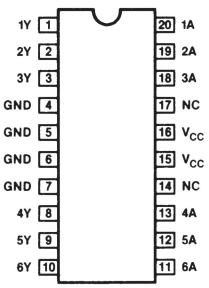
8-Input NAND Gate

11032



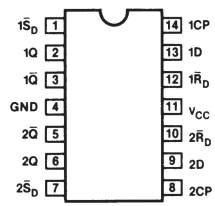
Quad 2-Input OR Gate

11034



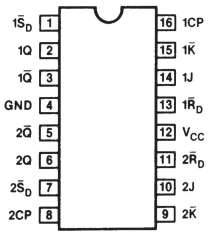
Hex Non-Inverter

11074



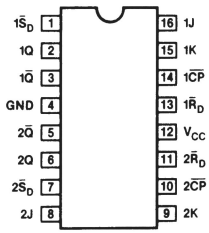
Dual D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger

11109



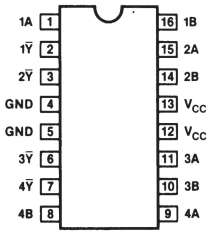
Dual JK Flip-Flop with Set and Reset; Positive-Edge Trigger

11112



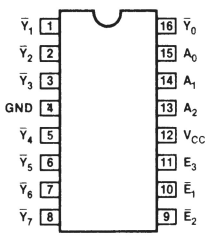
Dual JK Flip-Flop with Set and Reset; Negative-Edge Trigger

11132



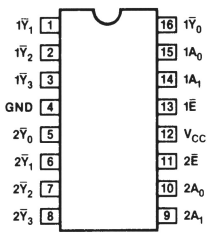
Quad 2-Input NAND Schmitt-Trigger

11138



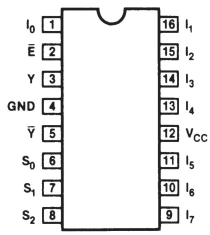
3-to-8 Line Decoder/Demultiplexer; Active Low

11139



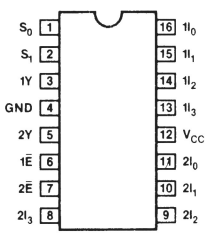
Dual 2-to-4 Line Decoder/Demultiplexer; Active Low

11151



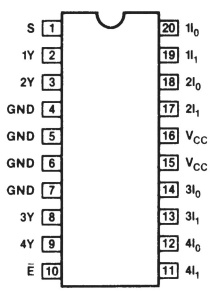
8-Input Multiplexer

11153



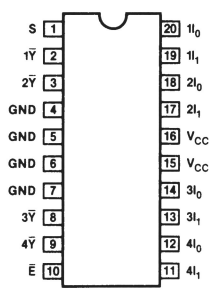
Dual 4-Input Multiplexer

11157



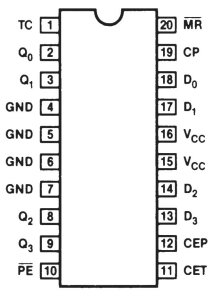
Quad 2-Input Multiplexer

11158



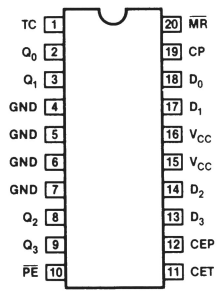
Quad 2-Input Multiplexer; Inverting

11160



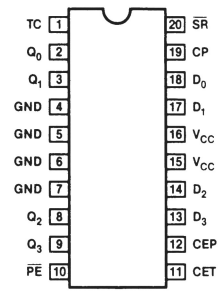
Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

11161



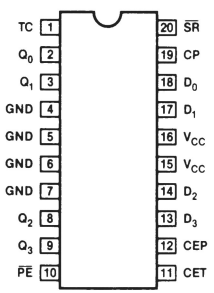
Synchronous Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset

11162



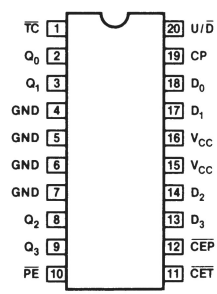
Synchronous Presettable Synchronous BCD Decade Counter; Synchronous Reset

11163



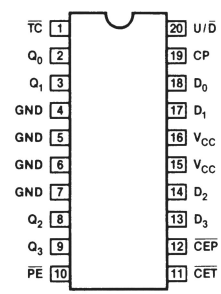
Synchronous Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset

11168



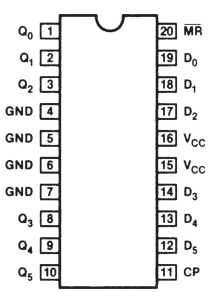
Synchronous Up/Down BCD Decade Counter

11169



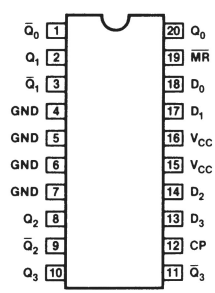
Synchronous Presettable 4-Bit Up/Down Binary Counter

11174



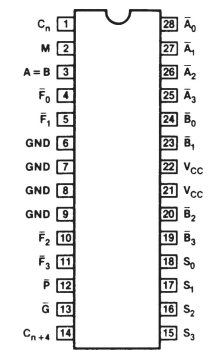
Hex D-Type Flip-Flop with Reset; Positive-Edge Trigger

11175



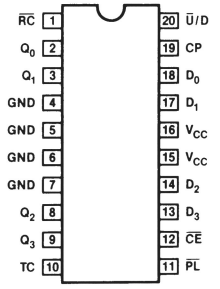
Quad D-Type Flip-Flop with Reset; Positive-Edge Trigger

11181



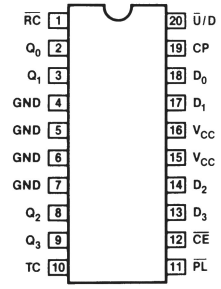
4-Bit Arithmetic Logic Unit

11190



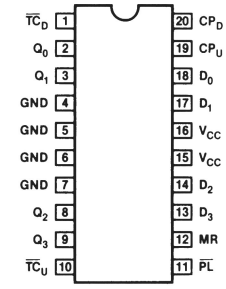
Asynchronous Presettable Synchronous Decade Up/Down Counter with Single Clock

11191



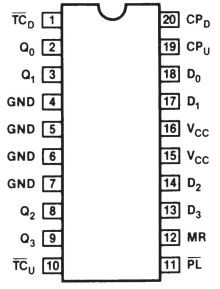
Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter with Single Clock

11192



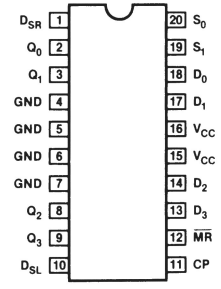
Asynchronous Presettable Synchronous BCD Decade Up/Down Counter with Dual Clock

11193



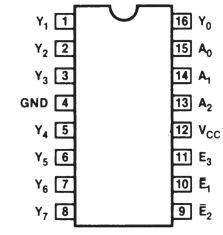
Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter with Dual Clock

11194



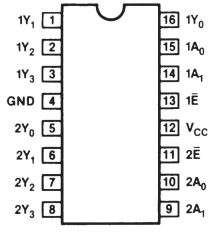
4-Bit Bidirectional Universal Shift Register

11238



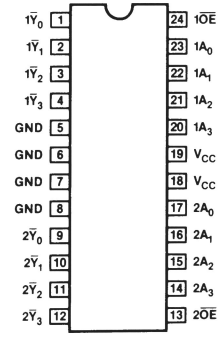
3-to-8 Line Decoder/Demultiplexer; Active High

11239



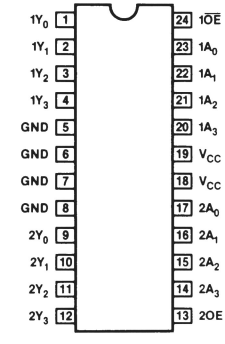
Dual 2-to-4 Line Decoder/Demultiplexer; Active High

11240



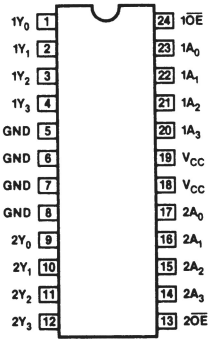
Octal Buffer/Line Driver; 3-State; Inverting

11241



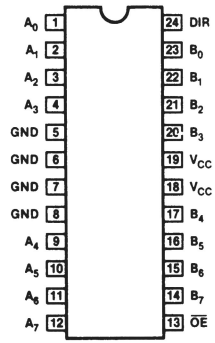
Octal Buffer/Line Driver; 3-State

11244



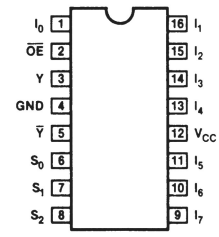
Octal Buffer/Line Driver; 3-State

11245



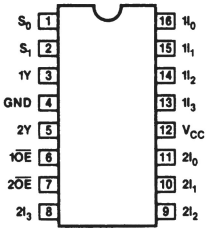
Octal Transceiver with Direction Pin; 3-State

11251



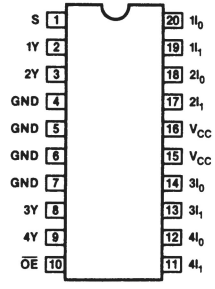
8-Input Multiplexer; 3-State

11253



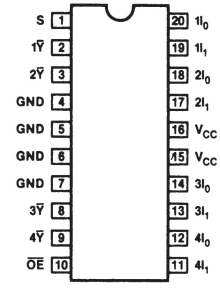
Dual 4-Input Multiplexer; 3-State

11257



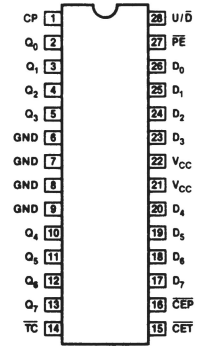
Quad 2-Input Multiplexer; 3-State

11258



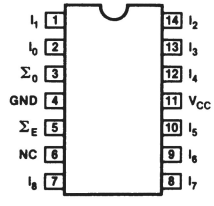
Quad 2-Input Multiplexer; 3-State; Inverting

11269



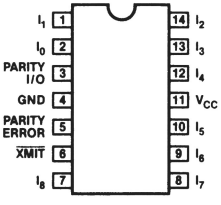
Synchronous Presettable 8-Bit Binary Up/Down Counter

11280



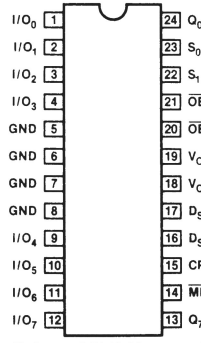
9-Bit Odd/Even Parity Generator/Checker

11286



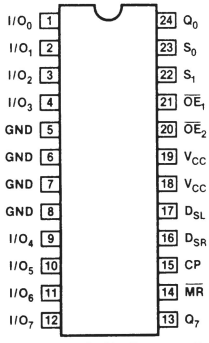
9-Bit Odd/Even Parity Generator/Checker with Bus Drive I/O Port

11299



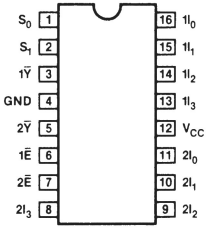
8-Input Universal Shift/Storage Register with Asynchronous Reset and Common I/O Pins

11323



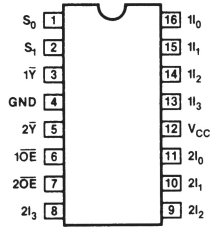
8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

11352



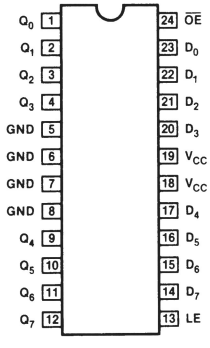
Dual 4-Input Multiplexer; Inverting

11353



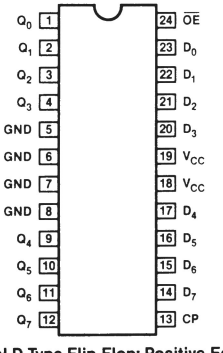
Dual 4-Input Multiplexer; 3-State; Inverting

11373



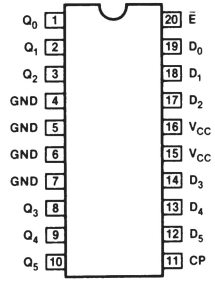
Octal D-Type Transparent Latch; 3-State

11374



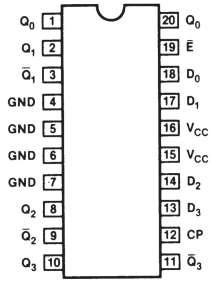
Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State

11378



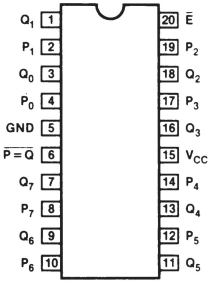
Hex D-Type Flip-Flop with Enable; Positive-Edge Trigger

11379



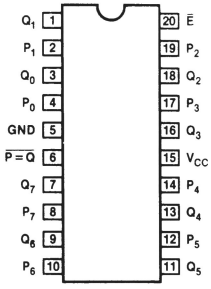
Quad D-Type Flip-Flop with Data Enable

11520



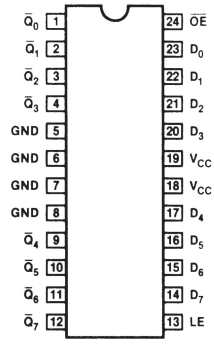
8-Bit Identity Comparator with Input Pull-Up

11521



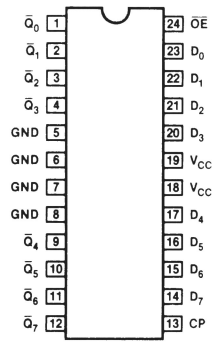
8-Bit Identity Comparator

11533



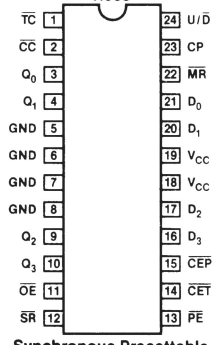
Octal D-Type Transparent Latch; 3-State; Inverting

11534



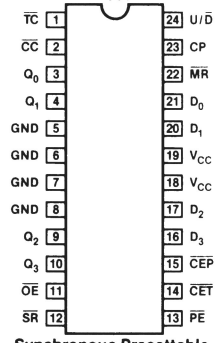
Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; Inverting

11568



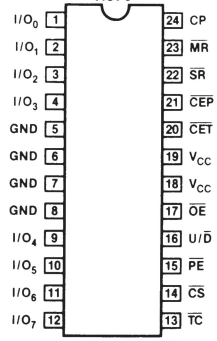
Synchronous Presettable BCD Decade Up/Down Counter with Synchronous and Asynchronous Reset

11569



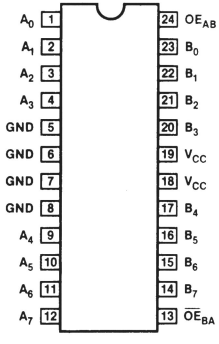
Synchronous Presettable 4-Bit Binary Up/Down Counter with Synchronous and Asynchronous Reset

11579



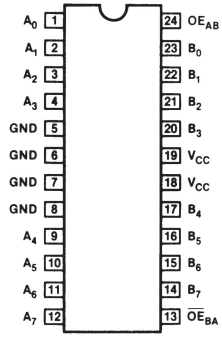
8-Bit Binary Up/Down Counter with Common I/O Pins; Synchronous and Asynchronous Reset; 3-State

11620



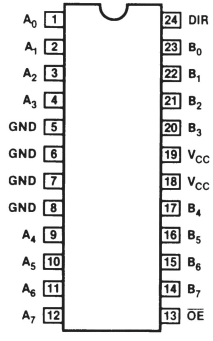
Octal Transceiver with Dual Enable; 3-State; Inverting

11623



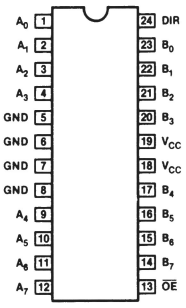
Octal Transceiver with Dual Enable; 3-State

11640



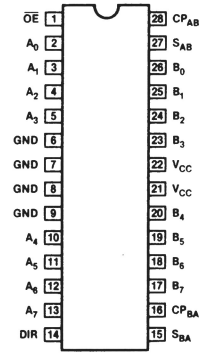
Octal Transceiver with Direction Pin; 3-State; Inverting

11643



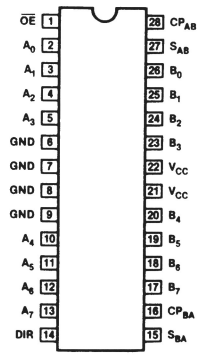
Octal Transceiver; 3-State; True/Inverting

11646



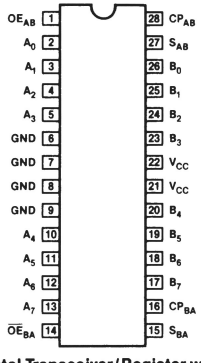
Octal Transceiver/Register with Direction Pin; 3-State

11648



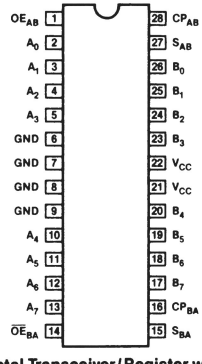
Octal Transceiver/Register with Direction Pin; 3-State; Inverting

11651



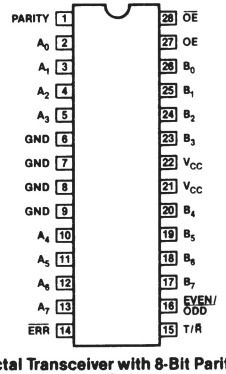
Octal Transceiver/Register with Dual Enable; 3-State; Inverting

11652



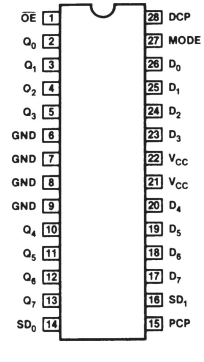
Octal Transceiver/Register with Dual Enable; 3-State

11657



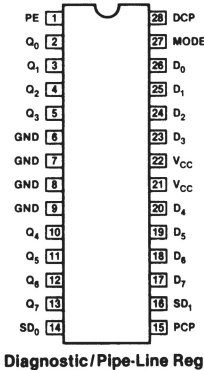
Octal Transceiver with 8-Bit Parity Checker/Generator

11818



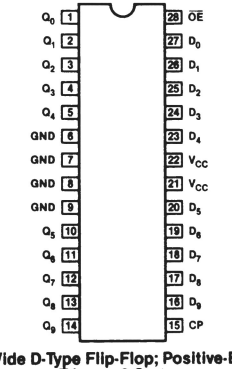
8-Bit Diagnostic/Pipe-Line Register

11819



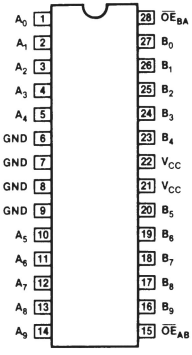
8-Bit Diagnostic/Pipe-Line Register with Parity Even Output

11821



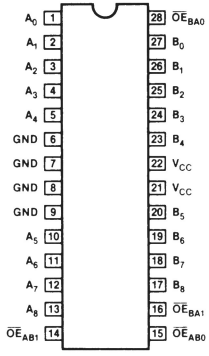
10-Wide D-Type Flip-Flop; Positive-Edge Trigger; 3-State

11862



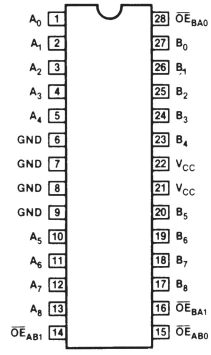
10-Wide Transceiver; 3-State; Inverting

11863



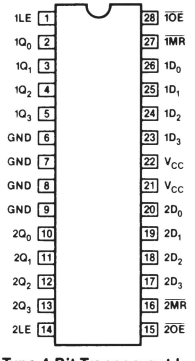
9-Wide Transceiver; 3-State

11864



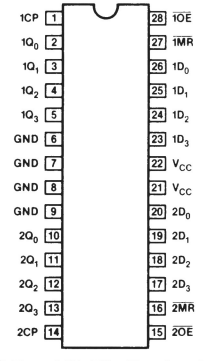
9-Wide Transceiver; 3-State; Inverting

11873



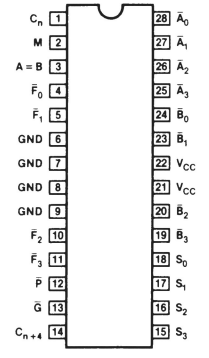
Dual D-Type 4-Bit Transparent Latch with Reset; 3-State

11874



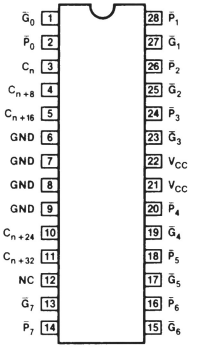
Dual D-Type 4-Bit Flip-Flop Latch with Reset; 3-State

11881



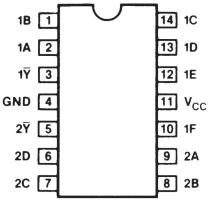
4-Bit Arithmetic Logic Unit with Status Check Register

11882



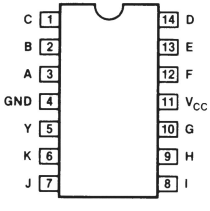
32-Bit Look-Ahead Carry Generator

11051



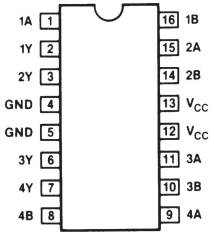
Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gate

11064



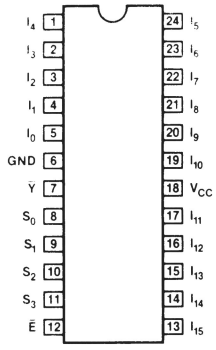
4-2-3-2-Input AND-OR-INVERT Gate

11086



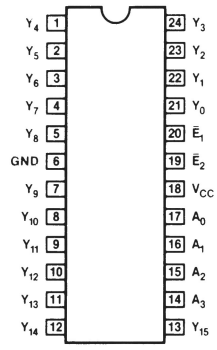
Quad 2-Input Exclusive-OR Gate

11150



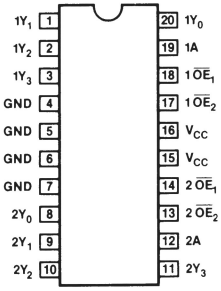
16-Input Multiplexer; 3-State; Inverting

11154



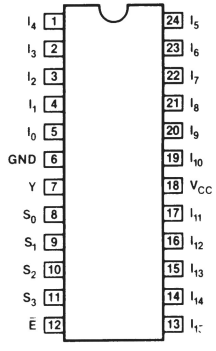
4-to-16 Line Decoder/Demultiplexer

11208



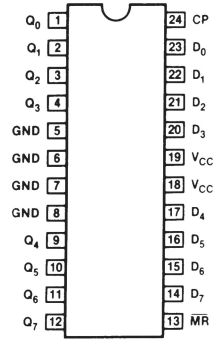
Dual 1-to-4 Line Driver; 3-State

11250



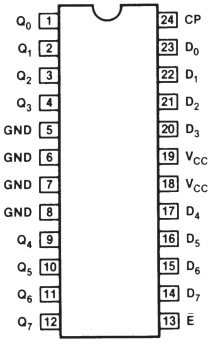
16-Input Multiplexer; 3-State

11273



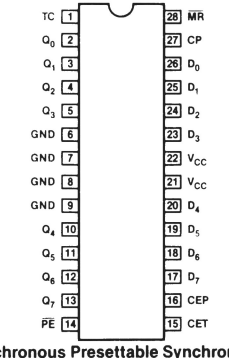
Octal D-Type Flip-Flop with Reset

11377



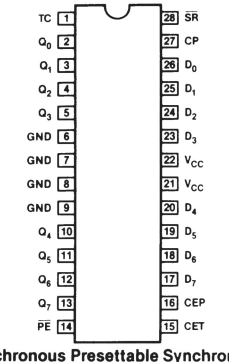
Octal D-Type Flip-Flop with Enable

11461



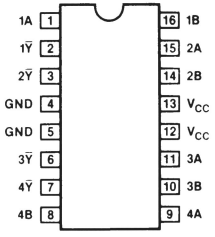
Synchronous Presettable Synchronous 8-Bit Binary Counter; Asynchronous Reset

11463



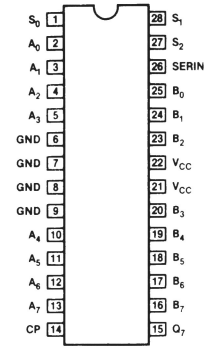
Synchronous Presettable Synchronous 8-Bit Binary Counter; Synchronous Reset

11810



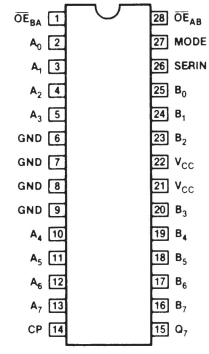
Quad 2-Input Exclusive-NOR Gate

11852



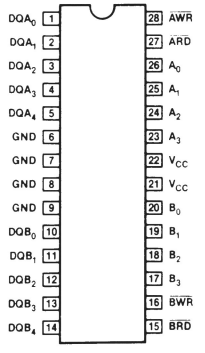
8-Bit Universal Transceiver Port Controller

11856



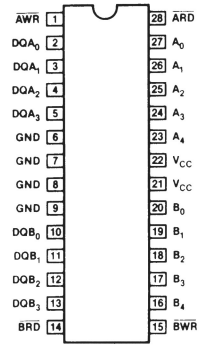
8-Bit Universal Transceiver Port Controller

11858



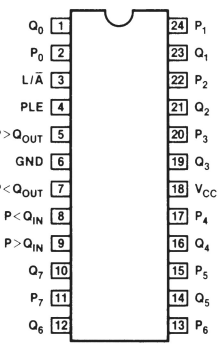
16-Word by 5-Bit Dual Port Register

11859



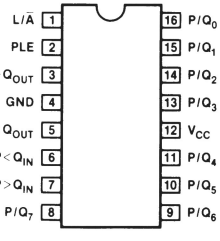
32-Word by 4-Bit Dual Port Register

11860



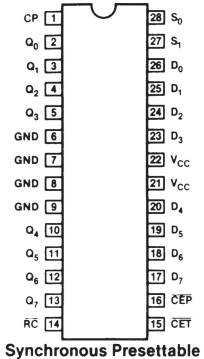
8-Bit Magnitude Comparator

11865



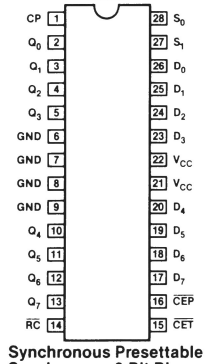
8-Bit Magnitude Comparator

11867



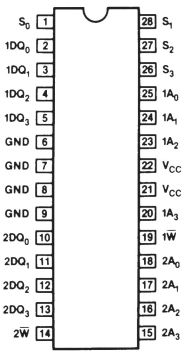
Synchronous Presettable Synchronous 8-Bit Binary Up/Down Counter; Asynchronous Reset

11869



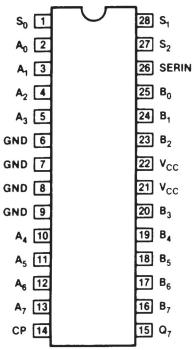
Synchronous Presettable Synchronous 8-Bit Binary Up/Down Counter; Synchronous Reset

11870



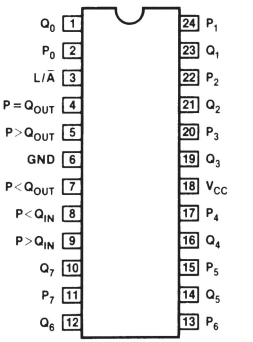
14-Word by 4-Bit Register

11877



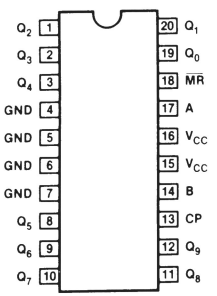
8-Bit Universal Transceiver Port Controller

11885



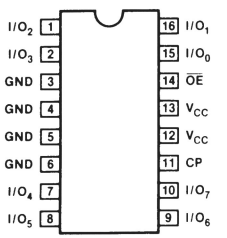
8-Bit Magnitude Comparator

11898



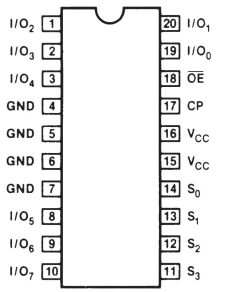
10-Bit Serial-In Parallel-Out Shift Register

11979



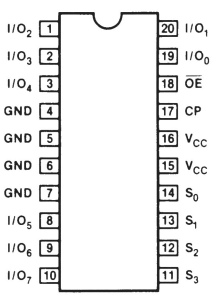
8-Bit Multiplexed I/O Read-Back Register

11980



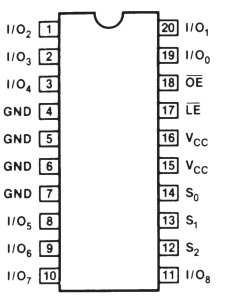
16-Word by 8-Bit Multiplexed I/O Read-Back Register

11981



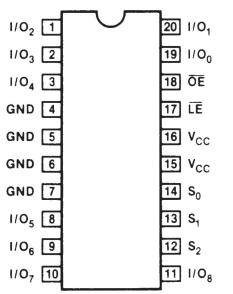
16-Word by 8-Bit Multiplexed I/O Read-Back Register with Address Latch

11987



8-Word by 9-Bit Multiplexed I/O Read-Back Register

11988



8-Word by 9-Bit Multiplexed I/O Read-Back Register with Address Latch

74AC/ACT11000

Quad 2-Input NAND Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11000 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11000 provides four separate 2-input NAND gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
		T_A = 25°C; GND = 0V	AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF; V_{CC} = 5V	4.7	6.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	33	23	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

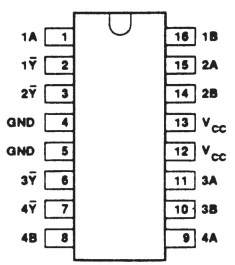
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

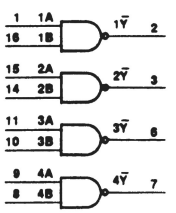
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11000N 74ACT11000N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11000D 74ACT11000D

PIN CONFIGURATION

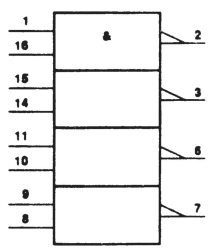
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	$n\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11000			74ACT11000			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11000				74ACT11000				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20, 19, 18, 13, 12, 11	1A - 6A	Data inputs
1, 2, 3, 8, 9, 10	$1\overline{Y}$ - $6\overline{Y}$	Data outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

INPUT	OUTPUT
nA	$n\overline{Y}$
L	H
H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11004			74ACT11004			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11004				74ACT11004				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 10	1A - 2A	Data inputs
1, 9	1B - 2B	Data inputs
13, 7	1C - 2C	Data inputs
12, 6	1D - 2D	Data inputs
3, 5	$1\overline{Y}$ - $2\overline{Y}$	Data outputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	$n\overline{Y}$
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11020			74ACT11020			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11020				74ACT11020				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11020					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5	6.4 6.4	8.6 9.2	1.5 1.5	9.4 10.1	ns

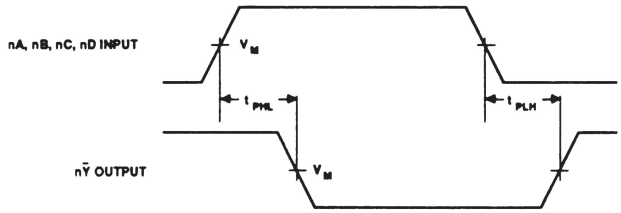
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11020					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5	4.3 4.4	6.3 6.7	1.5 1.5	6.7 7.3	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11020					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5	5.6 6.1	8.5 8.4	1.5 1.5	9.1 9.2	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nA, nB, nC, nD) to Output (n$\overline{Y}$) Propagation Delays

74AC/ACT11021
Dual 4-Input AND Gate
Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11021 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11021 provides two separate 4-input AND gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A, B, C, D to Y	C_L = 50pF; V_{CC} = 5V	5.1	6.1	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	38	37	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

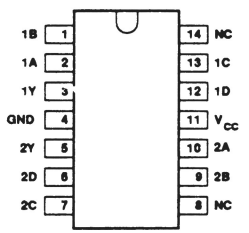
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

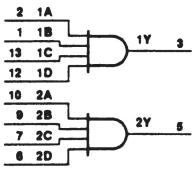
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11021N 74ACT11021N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11021D 74ACT11021D

PIN CONFIGURATION

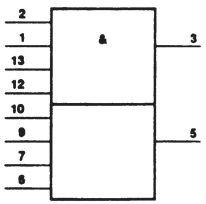
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 10	1A - 2A	Data inputs
1, 9	1B - 2B	Data inputs
13, 7	1C - 2C	Data inputs
12, 6	1D - 2D	Data inputs
3, 5	1Y - 2Y	Data outputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11021			74ACT11021			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11021				74ACT11021				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11021					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to nY	1	1.5 1.5	8.2 6.4	11.4 8.7	1.5 1.5	13.0 9.3	ns

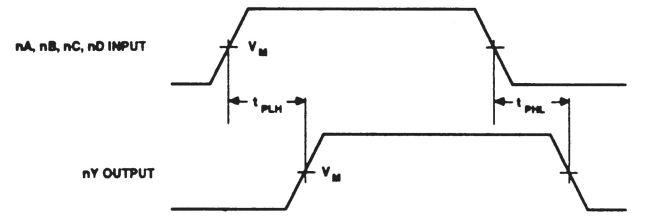
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11021					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to nY	1	1.5 1.5	5.6 4.6	7.8 6.5	1.5 1.5	8.8 6.9	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11021					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to nY	1	1.5 1.5	6.7 5.4	8.8 8.3	1.5 1.5	9.8 8.9	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nA, nB, nC, nD) to Output (nY) Propagation Delays

74AC/ACT11027

Triple 3-Input NOR Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11027 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11027 provides three separate 3-input NOR gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
		T_A = 25°C; GND = 0V	AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, C to $\overline{Y}$	C_L = 50pF; V_{CC} = 5V	4.4	5.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	24	27	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:

   f_I = input frequency in MHz, C_L = output load capacitance in pF,

   f_O = output frequency in MHz, V_{CC} = supply voltage in V,

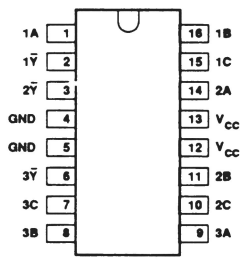
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

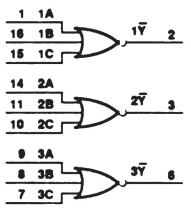
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11027N 74ACT11027N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11027D 74ACT11027D

PIN CONFIGURATION

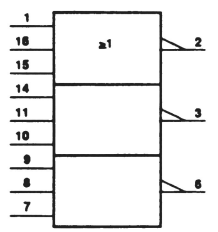
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 14, 9	1A - 3A	Data inputs
16, 11, 8	1B - 3B	Data inputs
15, 10, 7	1C - 3C	Data inputs
2, 3, 6	$1\overline{Y}$ - $3\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

INPUTS			OUTPUT
nA	nB	nC	$n\overline{Y}$
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11027			74ACT11027			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11027				74ACT11027				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11027					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	1	1.5 1.5	6.3 7.6	9.8 10.9	1.5 1.5	10.9 12.0	ns

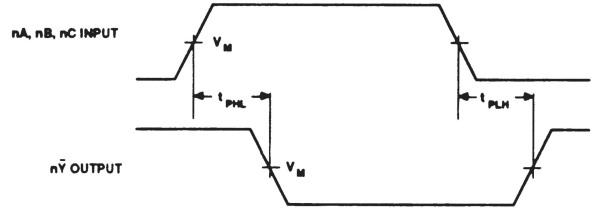
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11027					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	1	1.5 1.5	4.3 4.5	6.8 7.5	1.5 1.5	7.7 8.1	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11027					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC to n$\overline{Y}$	1	1.5 1.5	5.0 6.0	9.2 8.6	1.5 1.5	10.1 9.4	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nA, nB, nC) to Output (n$\overline{Y}$) Propagation Delays

74AC/ACT11030

8-Input NAND Gate

Product Specification

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: SSI

DESCRIPTION

The 74AC/ACT11030 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11030 provides one 8-input NAND gate function.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
		T_A = 25°C; GND = 0V	AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A through H to $\overline{Y}$	C_L = 50pF; V_{CC} = 5V	4.8	5.7	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	42	41	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

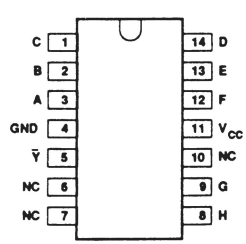
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

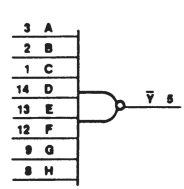
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11030N 74ACT11030N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11030D 74ACT11030D

PIN CONFIGURATION

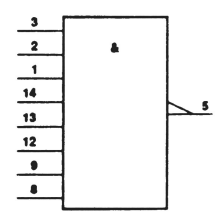
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
3, 2, 1, 14 13, 12, 9, 8	A, B, C, D, E, F, G, H	Data inputs
5	$\overline{Y}$	Data output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS	OUTPUT
A through H	$\overline{Y}$
All inputs H	L
One or more inputs L	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11030			74ACT11030			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11030				74ACT11030				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11030					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to $\overline{Y}$	1	1.5 1.5	6.9 6.4	9.1 8.8	1.5 1.5	9.9 9.8	ns

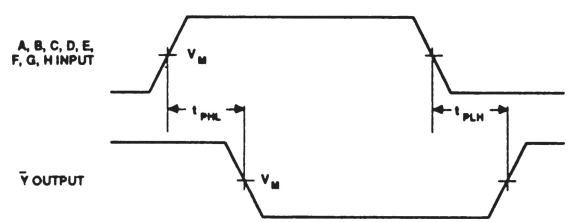
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11030					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to $\overline{Y}$	1	1.5 1.5	4.8 4.8	6.7 6.7	1.5 1.5	7.2 7.4	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11030					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D, E, F, G, H to $\overline{Y}$	1	1.5 1.5	5.4 5.9	8.1 7.8	1.5 1.5	8.5 8.7	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (A, B, C, D, E, F, G, H) to Output ($\overline{Y}$) Propagation Delays.

74AC/ACT11032

Quad 2-Input OR Gate

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11032 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11032 provides four separate 2-input OR gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
		T_A = 25°C; GND = 0V	AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, to Y	C_L = 50pF; V_{CC} = 5V	4.1	4.8	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	24	25	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

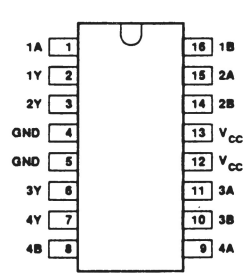
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

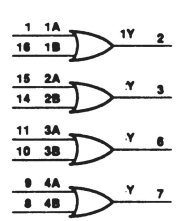
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11032N 74ACT11032N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11032D 74ACT11032D

PIN CONFIGURATION

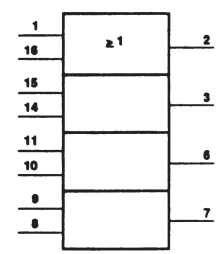
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	1Y - 4Y	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11032			74ACT11032			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11032				74ACT11032				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11002					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	6.3 5.4	8.7 7.4	1.5 1.5	9.7 8.0	ns

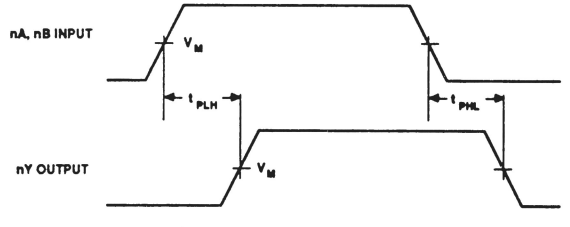
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11032					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	4.3 3.8	6.2 5.5	1.5 1.5	6.7 5.9	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11032					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	5.3 4.3	8.1 7.4	1.5 1.5	9.0 8.0	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nA, nB) to Output (nY) Propagation Delays

74AC/ACT11034

Hex Non-Inverter

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11034 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11034 provides six separate non-inverters.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A, B, to Y	C_L = 50pF; V_{CC} = 5V	4.0	5.7	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	27	29	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

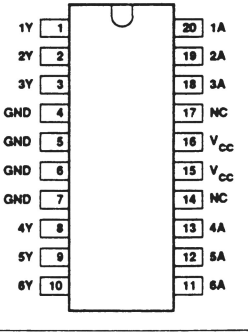
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

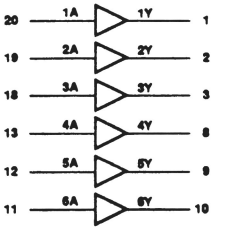
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11034N 74ACT11034N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11034D 74ACT11034D

PIN CONFIGURATION

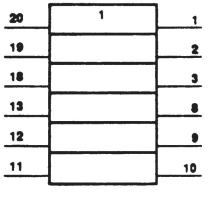
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20, 19, 18, 13, 12, 11	1A - 6A	Data inputs
1, 2, 3, 8, 9, 10	1Y - 6Y	Data outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	L
H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11034			74ACT11034			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11034				74ACT11034				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11034					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	5.7 5.5	9.1 8.3	1.5 1.5	10.1 9.2	ns

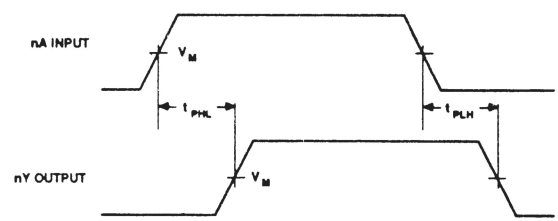
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11034					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	4.0 4.0	6.3 6.2	1.5 1.5	6.9 6.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11034					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	6.1 5.2	8.9 8.0	1.5 1.5	9.9 8.9	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V; V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nA) to Output (nY) Propagation Delays

74AC/ACT11074

Dual D-Type Flip-Flop w/Set and Reset; Positive-Edge Trigger

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11074 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11074 provides two D-type flip-flops with independent Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_n$) and Reset ($\overline{R}_n$) are asynchronous active-Low inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	C_L = 50pF; V_{CC} = 5V	5.2	5.9	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	30	30	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V	150	125	MHz

Note:

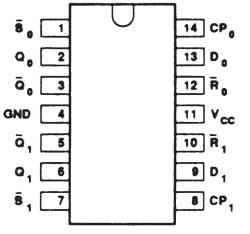
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

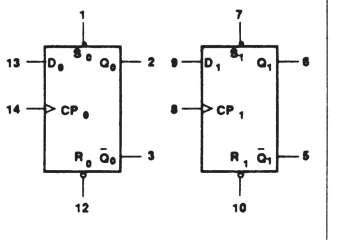
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11074N 74ACT11074N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11074D 74ACT11074D

PIN CONFIGURATION

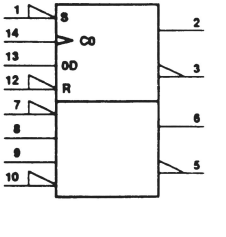
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
13, 9	D_0 - D_1	Data inputs
2, 6	Q_0 - Q_1	Data outputs
3, 5	$\overline{Q}_0$ - $\overline{Q}_1$	Data outputs (complements of Q_n outputs)
1, 7	$\overline{S}_0$ - $\overline{S}_1$	Set inputs (active Low)
12, 10	$\overline{R}_0$ - $\overline{R}_1$	Reset inputs (active Low)
14, 8	CP_0 - CP_1	Clock inputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

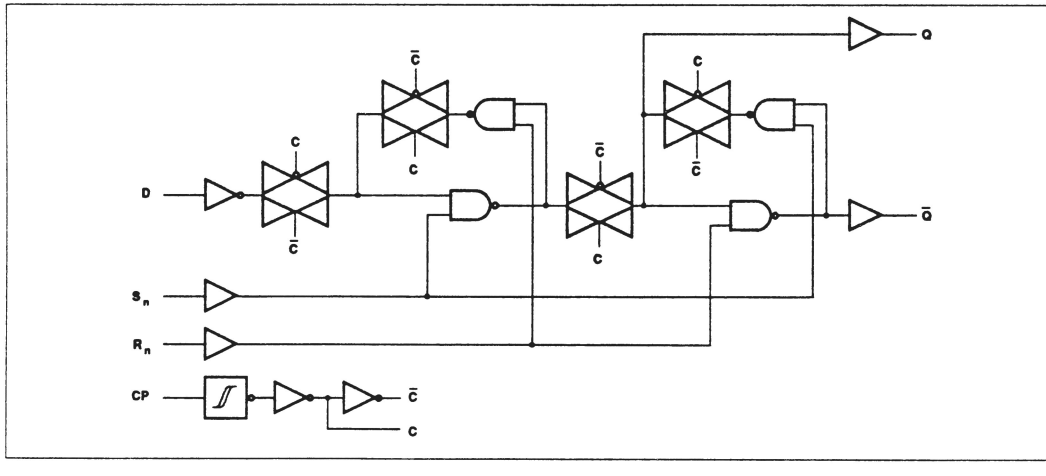
OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}$	$\overline{R}$	CP	D	Q	$\overline{Q}$
Asynchronous set	L	H	X	X	H	L
Asynchronous reset	H	L	X	X	L	H
Undetermined[1]	L	L	X	X	H	H
Load "1" (set)	H	H	↑	h	H	L
Load "0" (reset)	H	H	↑	l	L	H
No change – hold	H	H	L	X	Q_0	$\overline{Q}_0$

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

NOTE:

1. This configuration is nonstable; that is, it will not persist when either Set or Reset returns to its inactive (High) level.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11074			74ACT11074			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11074				74ACT11074				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11074					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	7.7 7.3	10.5 9.7	1.5 1.5	11.3 10.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	5.8 6.5	9.3 11.4	1.5 1.5	10.0 12.2	ns
t_S	Setup time, High or Low D_n to CP_n	1	5.0			5.0		ns
t_H	Hold time, High or Low CP_n to D_n	1	0			0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

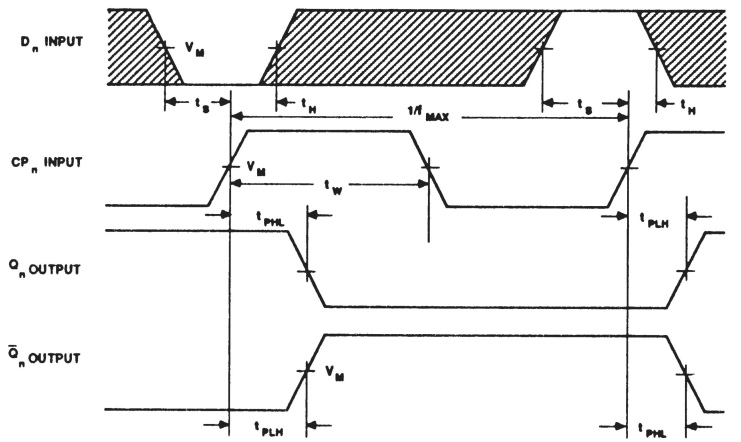
GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11074					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	5.4 5.0	7.5 6.9	1.5 1.5	8.2 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	4.2 4.7	6.6 8.2	1.5 1.5	7.1 9.0	ns
t_S	Setup time, High or Low D_n to CP_n	1	3.5			3.5		ns
t_H	Hold time, High or Low CP_n to D_n	1	0			0		ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

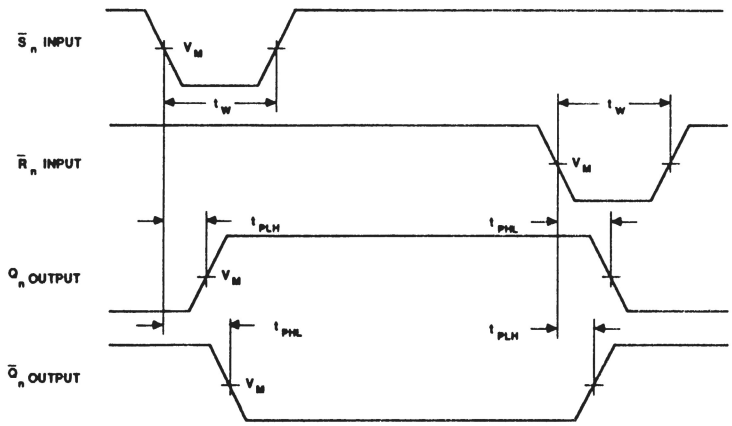
SYMBOL	PARAMETER	WAVEFORM	74ACT11074					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	6.0 5.7	8.5 8.0	1.5 1.5	9.4 8.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	5.7 6.6	8.9 11.3	1.5 1.5	9.6 12.5	ns
t_S	Setup time, High or Low D_n to CP_n	1	4.5			4.5		ns
t_H	Hold time, High or Low CP_n to D_n	1	0			0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	2.0			2.0		ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V

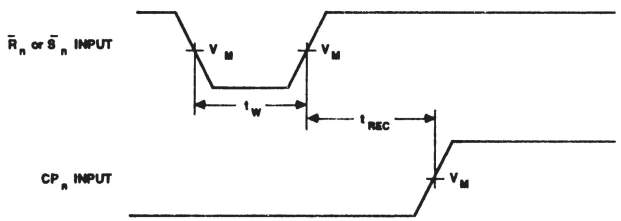


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 2. Waveforms Showing Set and Reset to Output Delays, Set and Reset Pulse Widths



Waveform 3. Waveforms Showing Recovery Time

74AC/ACT11086

Quad 2-Input Exclusive-OR Gate

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11086 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11086 provides four separate 2-input exclusive-OR gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
		T_A = 25°C; GND = 0V	AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, to Y	C_L = 50pF; V_{CC} = 5V	5.0	6.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	27	26	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

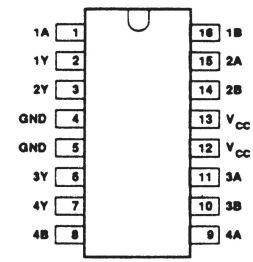
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

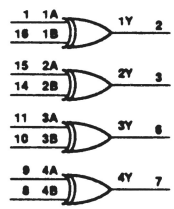
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11086N 74ACT11086N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11086D 74ACT11086D

PIN CONFIGURATION

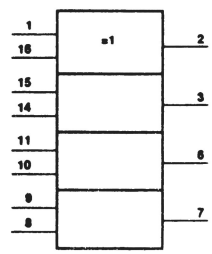
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	1Y - 4Y	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11086			74ACT11086			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11086				74ACT11086				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11086					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	7.0 6.0	9.0 7.5	1.5 1.5	10.1 8.1	ns

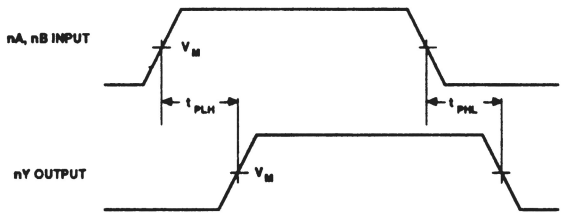
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11086					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	5.0 4.9	6.7 6.2	1.5 1.5	7.4 6.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11086					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to nY	1	1.5 1.5	6.6 6.4	8.7 8.1	1.5 1.5	9.4 8.7	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nA, nB) to Output (nY) Propagation Delays

74AC/ACT11109

Dual J-$\overline{K}$ Flip-Flop with Set and Reset; Positive Edge-Triggered

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11109 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11109 provides two J-$\overline{K}$ flip-flops with independent Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_n$) and Reset ($\overline{R}_n$) are asynchronous active-Low inputs and operate independently of the Clock input.

Information at the J and $\overline{K}$ inputs is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The J and $\overline{K}$ inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation. The J and K inputs may be tied together to allow operation as a D flip-flop.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	C_L = 50pF; V_{CC} = 5V	5.3	5.8	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	32	31	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V	125	125	MHz

Note:

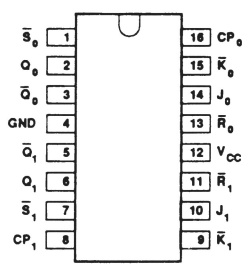
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

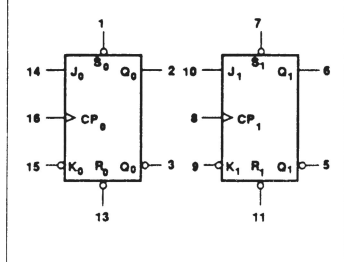
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11109N 74ACT11109N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11109D 74ACT11109D

PIN CONFIGURATION

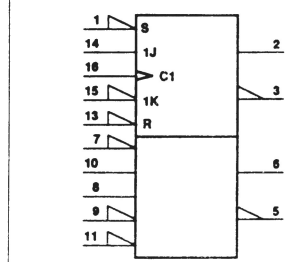
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 10	J_0 - J_1	Data inputs
15, 9	$\overline{K}_0$ - $\overline{K}_1$	Data inputs
2, 6	Q_0 - Q_1	Data outputs
3, 5	$\overline{Q}_0$ - $\overline{Q}_1$	Data outputs (complements of Q_n outputs)
1, 7	$\overline{S}_0$ - $\overline{S}_1$	Set inputs (active Low)
13, 11	$\overline{R}_0$ - $\overline{R}_1$	Reset inputs (active Low)
16, 8	CP_0 - CP_1	Clock inputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

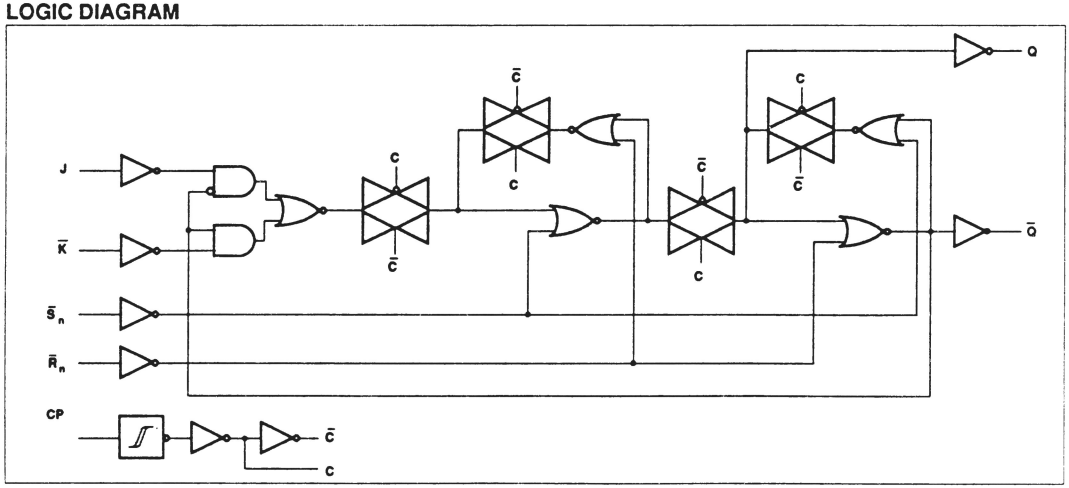
OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined[1]	L	L	X	X	X	H	H
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Toggle	H	H	↑	h	l	$\overline{q}$	q
No change – hold	H	H	L	X	X	Q_0	$\overline{Q}_0$

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

NOTE:

1. This configuration is nonstable; that is, it will not persist when either Set or Reset returns to its inactive (High) level.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11109			74ACT11109			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11109				74ACT11109				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11109					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	70	100		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	8.0 7.5	11.4 10.5	1.5 1.5	12.7 11.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	6.5 8.0	9.0 12.6	1.5 1.5	9.9 13.7	ns
t_S	Setup time, High or Low J_n or $\overline{K}_n$ to CP_n	1	5.5			5.5		ns
t_H	Hold time, High or Low CP_n to J_n or $\overline{K}_n$	1	0			0		ns
t_W	Clock pulse width High or Low	1	7.2			7.2		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	2.5			2.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11109					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	5.5 5.0	7.9 7.3	1.5 1.5	8.8 8.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	4.5 5.0	6.5 8.6	1.5 1.5	7.1 9.6	ns
t_S	Setup time, High or Low J_n or $\overline{K}_n$ to CP_n	1	4.5			4.5		ns
t_H	Hold time, High or Low CP_n to J_n or $\overline{K}_n$	1	0			0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	2.0			2.0		ns

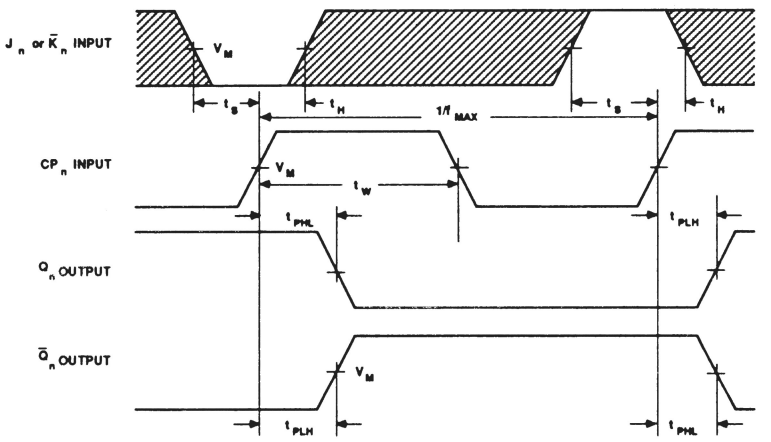
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11109					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n, $\overline{Q}_n$	1	1.5 1.5	6.0 5.5	8.3 7.6	1.5 1.5	9.1 8.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_n$, $\overline{R}_n$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	5.5 6.0	8.6 10.8	1.5 1.5	9.2 11.8	ns
t_S	Setup time, High or Low J_n or $\overline{K}_n$ to CP_n	1	5.5			5.5		ns
t_H	Hold time, High or Low CP_n to J_n or $\overline{K}_n$	1	0			0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{S}_n$ or $\overline{R}_n$ pulse width, Low	2	5.5			5.5		ns
t_{REC}	Recovery time $\overline{S}_n$ or $\overline{R}_n$ to CP_n	3	2.0			2.0		ns

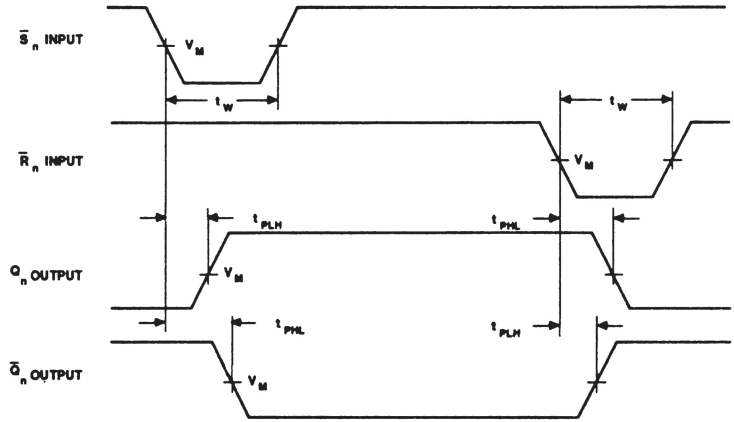
AC WAVEFORMS

AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V

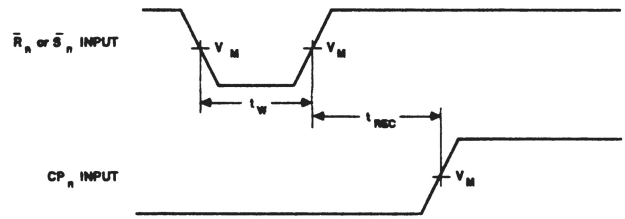


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 2. Waveforms Showing Set and Reset to Output Delays, Set and Reset Pulse Widths



Waveform 3. Waveforms Showing Recovery Time

74AC/ACT11112

Dual J-K Flip-Flop with Set and Reset; Negative Edge-Triggered

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11112 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11112 provides two J-K flip-flops with independent Data, Clock, Set and Reset inputs, and complementary nQ and $n\overline{Q}$ outputs.

Set ($n\overline{S}_D$) and Reset ($n\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock inputs.

Information at the J and K inputs is transferred to the outputs on the High-to-Low transition of the clock pulse. The J and K inputs must be stable one set-up time prior to the High-to-Low clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay $n\overline{CP}$ to nQ or $n\overline{Q}$	C_L = 50pF; V_{CC} = 5V	4.5	6.7	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	37	39	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta V/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V	180	150	MHz

Note:

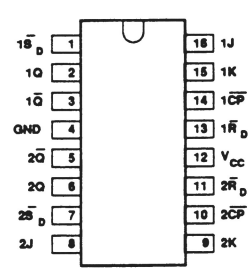
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

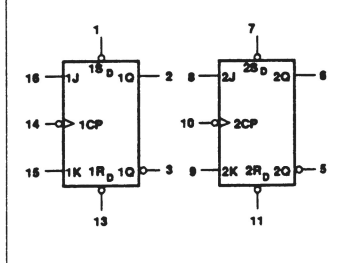
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11112N 74ACT11112N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11112D 74ACT11112D

PIN CONFIGURATION

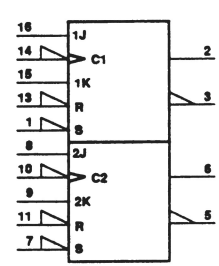
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
16, 8	1J - 2J	Data inputs
15, 9	1K - 2K	Data inputs
2, 6	1Q - 2Q	Data outputs
3, 5	$\overline{1Q}$ - $\overline{2Q}$	Data outputs (complements of Q_n outputs)
1, 7	$1\overline{S}_D$ - $2\overline{S}_D$	Set inputs (active Low)
13, 11	$1\overline{R}_D$ - $2\overline{R}_D$	Reset inputs (active Low)
14, 10	$1\overline{CP}$ - $2\overline{CP}$	Clock inputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

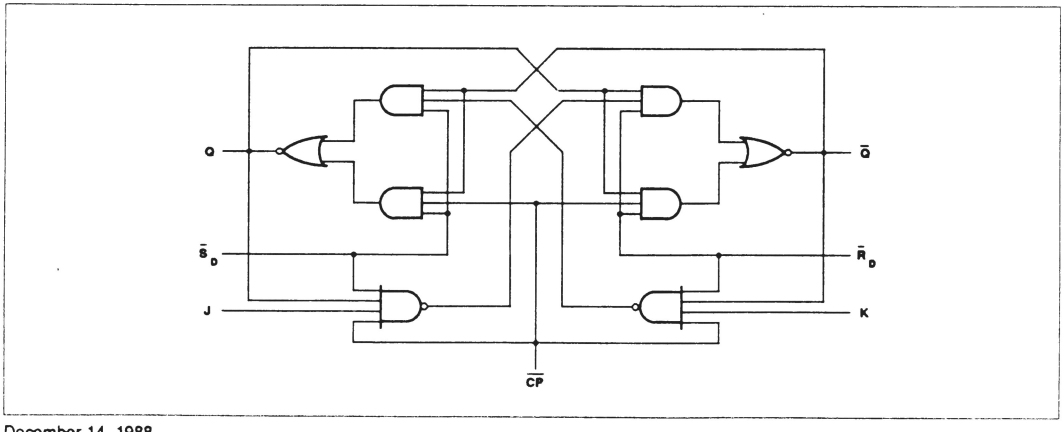
OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined[1]	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (reset)	H	H	↓	l	h	L	H
Load "1" (set)	H	H	↓	h	l	H	L
No change – hold	H	H	↓	l	l	q	$\overline{q}$
No change – hold	H	H	H	X	X	Q	$\overline{Q}$

H = High voltage level steady state
h = High voltage level one set-up time prior to the High-to-Low clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the High-to-Low clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition
↓ = High-to-Low clock transition

NOTE:

1. This configuration is nonstable; that is, it will not persist when either Set or Reset returns to its inactive (High) level.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11112			74ACT11112			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11112				74ACT11112				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current; TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11112					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	80	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay $n\overline{CP}$ to nQ, $n\overline{Q}$	1	1.5 1.5	6.2 6.6	8.2 8.5	1.5 1.5	9.0 9.3	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{S}_D$, $n\overline{R}_D$ to nQ, $n\overline{Q}$	2	1.5 1.5	5.7 7.7	7.7 10.0	1.5 1.5	8.3 10.9	ns
t_S	Setup time, High or Low nJ or nK to $n\overline{CP}$	1	6.0			6.0		ns
t_H	Hold time, High or Low $n\overline{CP}$ to nJ or nK	1	0			0		ns
t_W	Clock pulse width High or Low	1	6.3			6.3		ns
t_W	$n\overline{S}_D$ or $n\overline{R}_D$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $n\overline{S}_D$ or $n\overline{R}_D$ to $n\overline{CP}$	3	1.5			1.5		ns

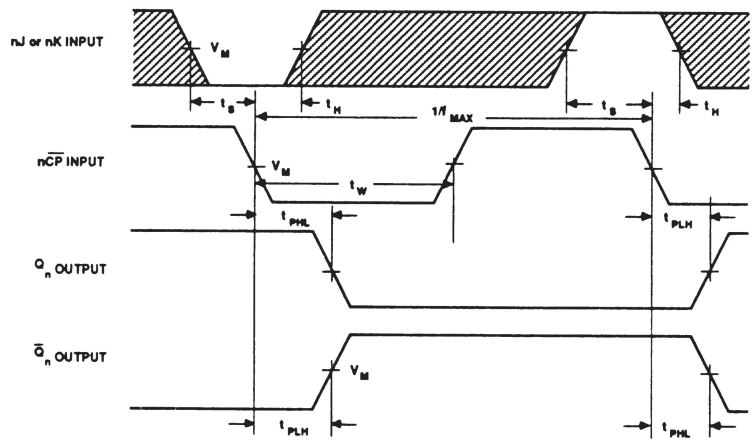
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11112					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	180		125		MHz
t_{PLH} t_{PHL}	Propagation delay $n\overline{CP}$ to nQ, $n\overline{Q}$	1	1.5 1.5	4.2 4.7	5.8 6.2	1.5 1.5	6.4 6.9	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{S}_D$, $n\overline{R}_D$ to nQ, $n\overline{Q}$	2	1.5 1.5	3.9 5.4	5.5 7.1	1.5 1.5	5.9 7.8	ns
t_S	Setup time, High or Low nJ or nK to $n\overline{CP}$	1	4.0			4.0		ns
t_H	Hold time, High or Low $n\overline{CP}$ to nJ or nK	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$n\overline{S}_D$ or $n\overline{R}_D$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $n\overline{S}_D$ or $n\overline{R}_D$ to $n\overline{CP}$	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

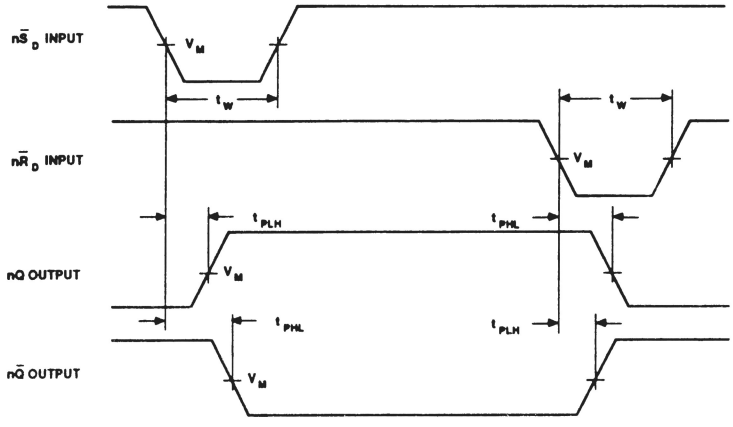
SYMBOL	PARAMETER	WAVEFORM	74ACT11112					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay $n\overline{CP}$ to nQ , $n\overline{Q}$	1	1.5 1.5	6.6 6.8	8.2 8.4	1.5 1.5	9.0 9.3	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{S}_D$, $n\overline{R}_D$ to nQ , $n\overline{Q}$	2	1.5 1.5	5.9 7.4	7.6 9.1	1.5 1.5	8.1 9.9	ns
t_S	Setup time, High or Low nJ or nK to $n\overline{CP}$	1	4.0			4.0		ns
t_H	Hold time, High or Low $n\overline{CP}$ to nJ or nK	1	1.0			1.0		ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$n\overline{S}_D$ or $n\overline{R}_D$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $n\overline{S}_D$ or $n\overline{R}_D$ to $n\overline{CP}$	3	2.0			2.0		ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V

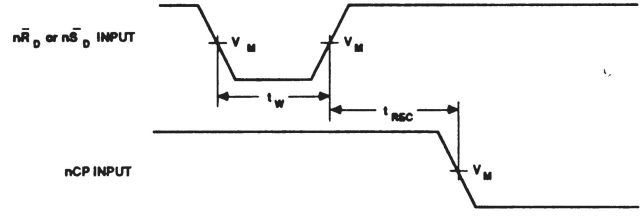


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 2. Waveforms Showing Set and Reset to Output Delays, Set and Reset Pulse Widths



Waveform 3. Waveforms Showing Recovery Time

74AC/ACT11132

Quad 2-Input NAND Schmitt-Trigger

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11132 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11132 provides four separate 2-input NAND gate functions which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF; V_{CC} = 5V	5.2		ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	27		pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5		pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500		mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	100		ns/V

Note:

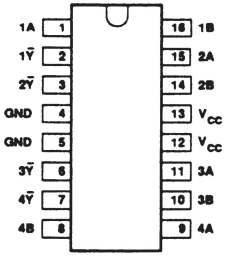
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

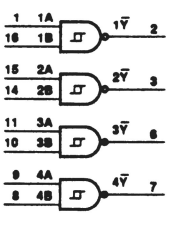
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11132N 74ACT11132N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11132D 74ACT11132D

PIN CONFIGURATION

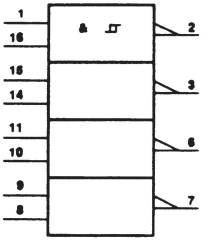
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	$n\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11132			74ACT11132			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	0		100	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11132				74ACT11132				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive-going threshold			3.0		2.2		2.2					V
				4.5		3.2		3.2		2.0		2.0	
				5.5		3.9		3.9		2.0		2.0	
V_{T-}	Negative-going threshold			3.0	0.5		0.5						V
				4.5	0.9		0.9			0.8		0.8	
				5.5	1.1		1.1			0.8		0.8	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)			3.0	0.3	1.2	0.3	1.2					V
				4.5	0.4	1.4	0.4	1.4	0.4	1.2	0.4	1.2	
				5.5	0.5	1.6	0.5	1.6	0.4	1.2	0.4	1.2	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11132					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	6.9 7.6	9.0 9.5	1.5 1.5	9.7 10.4	ns

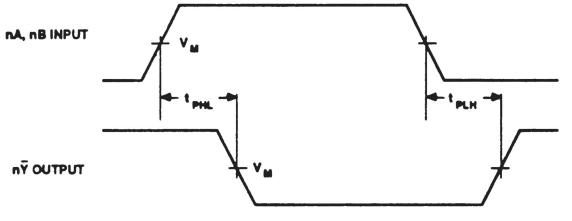
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11132					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	4.9 5.4	6.6 7.0	1.5 1.5	7.1 7.6	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11132					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nA, nB) to Output (n$\overline{Y}$) Propagation Delays

74AC/ACT11138

3-to-8 Line Decoder/ Demultiplexer; Active-Low

Preliminary Specification

FEATURES

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Inverting outputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11138 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11138 decoders accept three binary weighted inputs (A_0, A_1, A_2) and when enabled, provide eight mutually exclusive, active-Low outputs ($\overline{Y}_0$ - $\overline{Y}_7$). The devices feature three enable inputs; two active-Low ($\overline{E}_1$, $\overline{E}_2$) and one active-High (E_3). Every output will be High unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enable function allows easy parallel expansion of the devices to a 1-of-32 (5 lines to 32 lines) decoder with just four '11138's and one inverter.

The devices can be used as eight output demultiplexers by using one of the active-Low enable inputs as the data input and the remaining enable inputs as strobes.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF; V_{CC} = 5V	6.0	6.1	ns
C_{PD}	Power dissipation capacitance[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	56	61	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

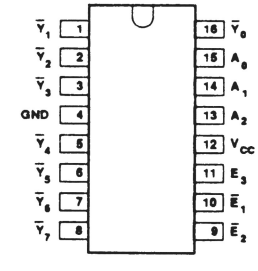
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

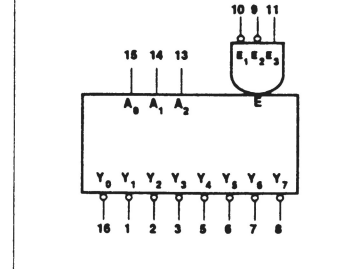
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11138N 74ACT11138N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11138D 74ACT11138D

PIN CONFIGURATION

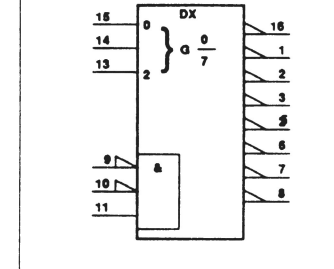
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



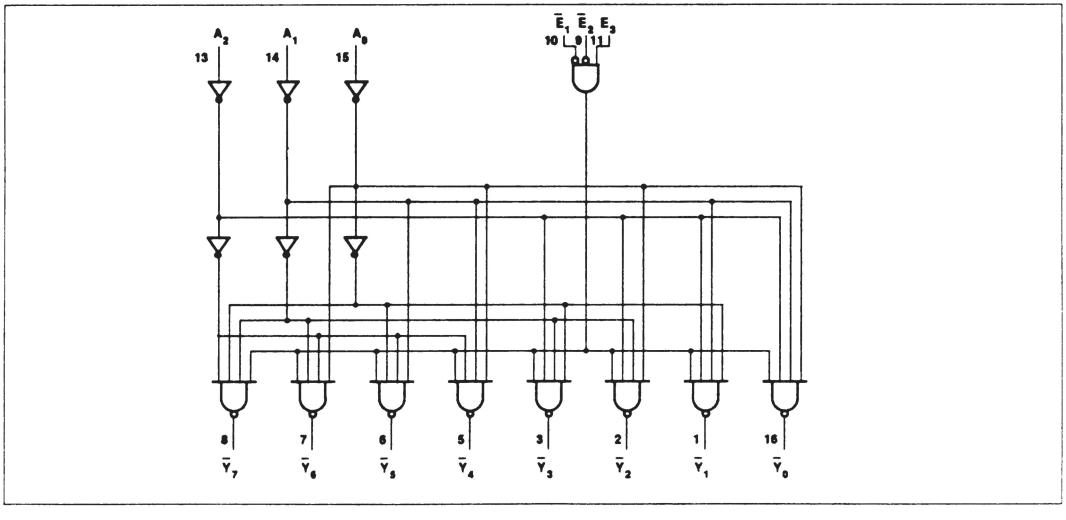
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14, 13	A_0 to A_2	Address inputs
10, 9	$\overline{E}_1$, $\overline{E}_2$	Enable inputs (active Low)
11	E_3	Enable input (active High)
16, 8, 7, 6, 5, 3, 2, 1	$\overline{Y}_0$ to $\overline{Y}_7$	Outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11138			74ACT11138			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11138				74ACT11138				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11138					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	8.3 8.9	10.2 10.9	1.5 1.5	11.4 12.2	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to $\overline{Y}_n$	2	1.5 1.5	7.2 7.3	9.2 9.4	1.5 1.5	10.2 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	2	1.5 1.5	8.2 8.3	10.4 10.4	1.5 1.5	11.5 11.6	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

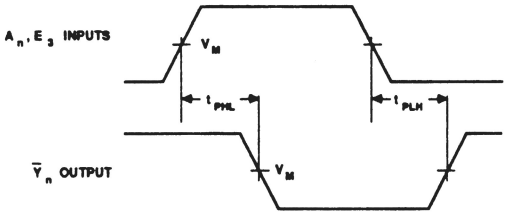
SYMBOL	PARAMETER	WAVEFORM	74AC11138					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	5.7 6.2	7.3 7.9	1.5 1.5	8.1 8.8	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to $\overline{Y}_n$	2	1.5 1.5	5.1 5.2	6.9 6.9	1.5 1.5	7.5 7.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	2	1.5 1.5	5.8 5.6	7.6 7.5	1.5 1.5	8.3 8.3	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

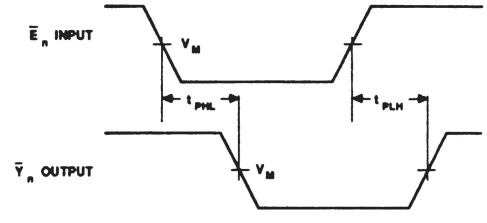
SYMBOL	PARAMETER	WAVEFORM	74ACT11138					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	5.7 6.4	8.1 8.0	1.5 1.5	8.8 9.1	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to $\overline{Y}_n$	2	1.5 1.5	5.3 5.8	7.5 7.5	1.5 1.5	8.1 8.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	2	1.5 1.5	6.2 5.8	8.1 8.0	1.5 1.5	8.8 8.9	ns

AC WAVEFORMS

AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V

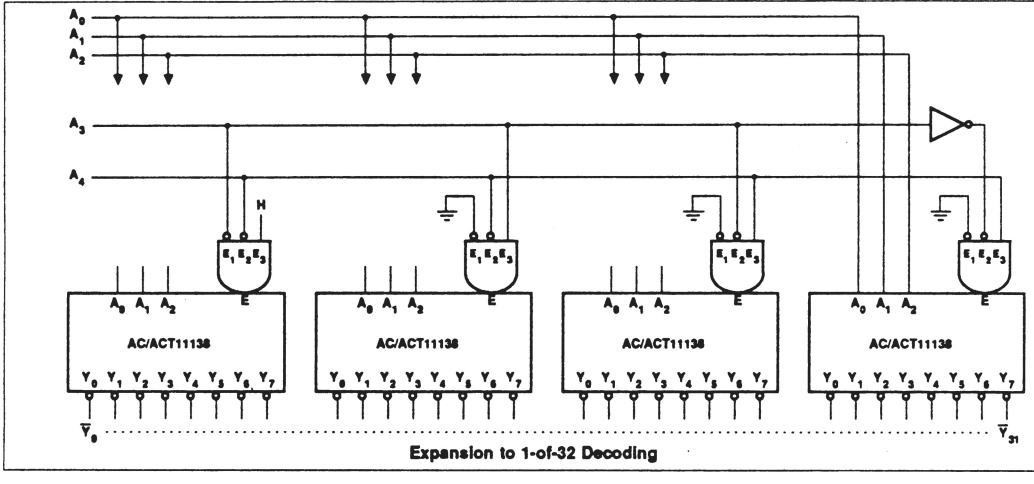


Waveform 1. Waveforms Showing the Inputs (A_n, E_3) to Output ($\overline{Y}_n$) Propagation Delays



Waveform 2. Waveforms Showing the Input ($\overline{E}_n$) to Output ($\overline{Y}_n$) Propagation Delays

APPLICATION



Expansion to 1-of-32 Decoding

74AC/ACT11151
8-Input Multiplexer

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11151 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11151 provides an 8-to-1 multiplexer with three select lines and a common enable. The state of the Select (S_n) inputs determines the particular input line from which the data comes. The Enable ($\overline{E}$) input is active-Low. When $\overline{E}$ is High, the Y output is forced Low and the $\overline{Y}$ is forced High regardless of all other input conditions.

The device is the logic implementation of a single pole, 8 position switch where the position of the switch is determined by the logic levels supplied to the Select inputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay I_n to Y	C_L = 50pF; V_{CC} = 5V	4.8	6.6	ns
C_{PD}	Power dissipation capacitance[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	52	56	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
$\Delta t/\Delta v$	Maximum input rise or fall rate; Data inputs	C_L = 50pF; V_{cc} = 5.5V at -55°C	10	10	ns/V

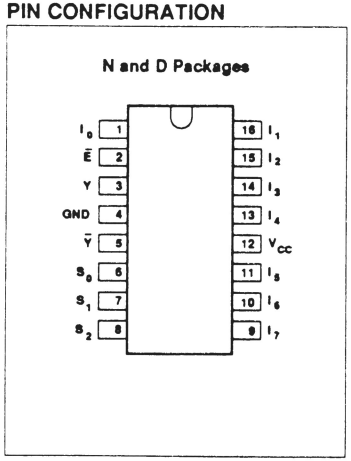
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

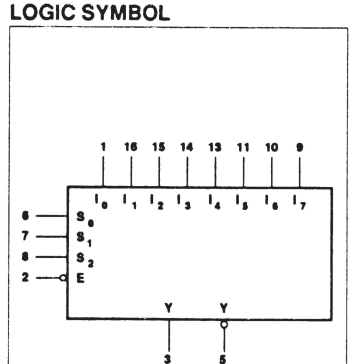
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11151N 74ACT11151N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11151D 74ACT11151D

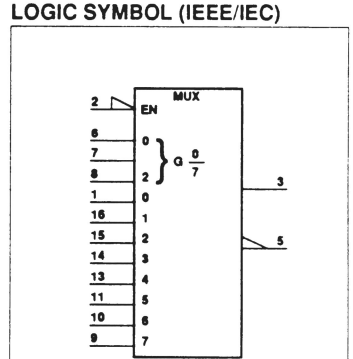
PIN CONFIGURATION



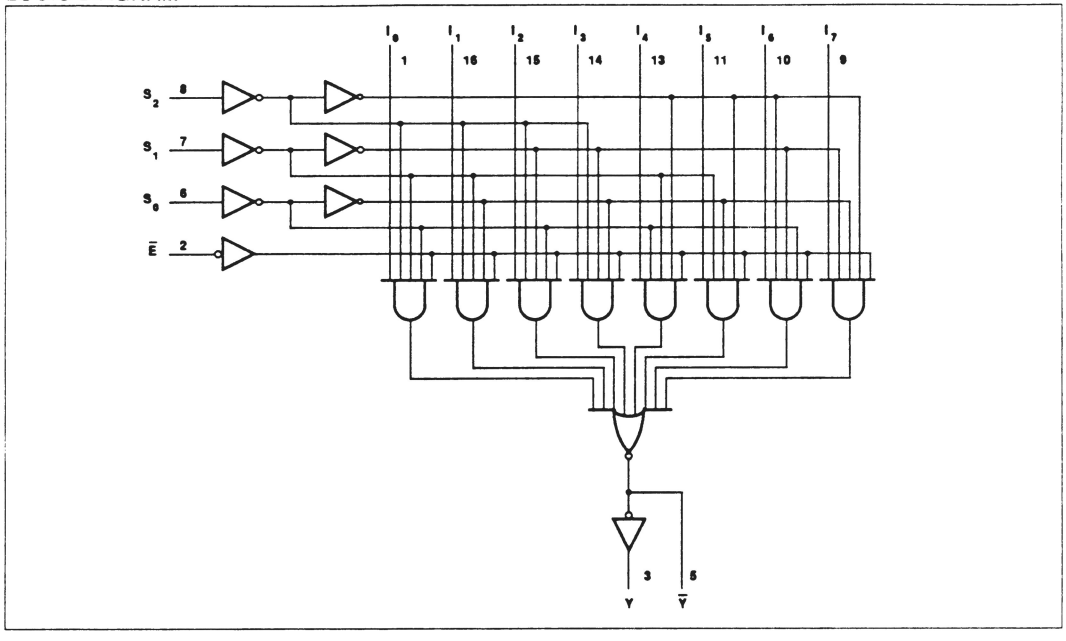
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
6, 7, 8	S_n	Select inputs
2	$\overline{E}$	Output enable input
1, 16, 15, 14 13, 11, 10, 9	$I_0 - I_7$	Data inputs
3, 5	Y, $\overline{Y}$	Data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	E	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11151			74ACT11151			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11151				74ACT11151				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11151					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	2	1.5 1.5	7.2 7.3	8.5 8.9	1.5 1.5	9.4 9.6	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	2	1.5 1.5	7.0 7.0	8.3 8.4	1.5 1.5	9.1 9.1	ns
t_{PLH} t_{PHL}	Propagation delay S to Y	2	1.5 1.5	10.1 10.0	11.7 12.1	1.5 1.5	12.8 13.1	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$	2	1.5 1.5	9.8 9.9	11.6 11.7	1.5 1.5	12.6 12.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	1	1.5 1.5	4.5 4.6	5.7 6.0	1.5 1.5	6.2 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	1	1.5 1.5	5.2 5.0	6.4 6.3	1.5 1.5	6.8 6.8	ns

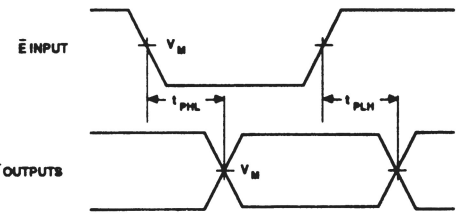
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11151					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	2	1.5 1.5	4.7 4.8	6.0 6.1	1.5 1.5	6.6 6.6	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	2	1.5 1.5	4.5 4.7	5.7 5.9	1.5 1.5	6.2 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S to Y	2	1.5 1.5	6.4 6.5	7.8 8.0	1.5 1.5	8.5 8.8	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$	2	1.5 1.5	6.3 6.3	7.6 7.7	1.5 1.5	8.3 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	1	1.5 1.5	3.1 3.3	4.3 4.6	1.5 1.5	4.6 5.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	1	1.5 1.5	3.7 3.5	4.9 4.6	1.5 1.5	5.3 5.0	ns

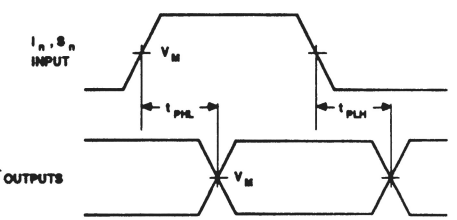
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11151					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	2	1.5 1.5	6.3 6.9	7.7 8.4	1.5 1.5	8.3 9.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	2	1.5 1.5	6.2 5.7	7.7 7.0	1.5 1.5	8.2 7.7	ns
t_{PLH} t_{PHL}	Propagation delay S to Y	2	1.5 1.5	9.0 8.3	10.5 10.1	1.5 1.5	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}$	2	1.5 1.5	7.8 8.4	9.4 10.0	1.5 1.5	10.3 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y	1	1.5 1.5	4.9 4.4	6.3 5.7	1.5 1.5	6.6 6.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$	1	1.5 1.5	5.0 5.3	6.2 6.7	1.5 1.5	6.7 7.1	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Enable Input ($\overline{E}$) to Output (Y, $\overline{Y}$) Propagation Delays



Waveform 2. Waveforms Showing the Data Inputs (nI_0, nI_1) and Select Input (S_n) to Output (Y, $\overline{Y}$) Propagation Delays

74AC/ACT11158

Quad 2-Input Multiplexer; INV

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11158 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11158 provides four 2-to-1 multiplexers with a common selector and a common enable. The state of the Select (S) input determines the particular register from which the data comes. The Enable ($\overline{E}$) input is active-Low. When $\overline{E}$ is High, all of the inverting outputs ($\overline{Y}$) are forced High regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	C_L = 50pF; V_{CC} = 5V	3.9		ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	33		pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5		pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500		mA
$\Delta t/\Delta v$	Maximum input rise or fall rate; Data inputs	C_L = 50pF; V_{cc} = 5.5V at -55°C	10		ns/V

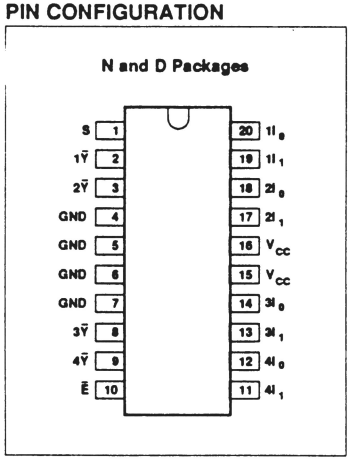
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

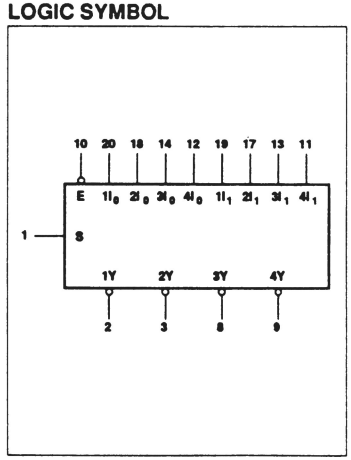
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11158N 74ACT11158N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11158D 74ACT11158D

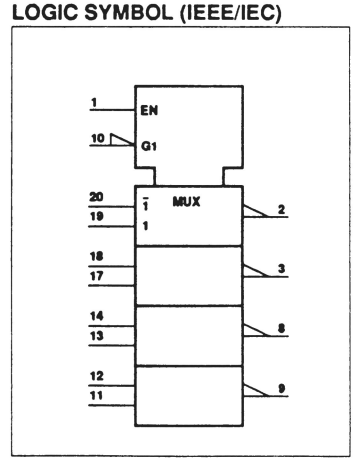
PIN CONFIGURATION



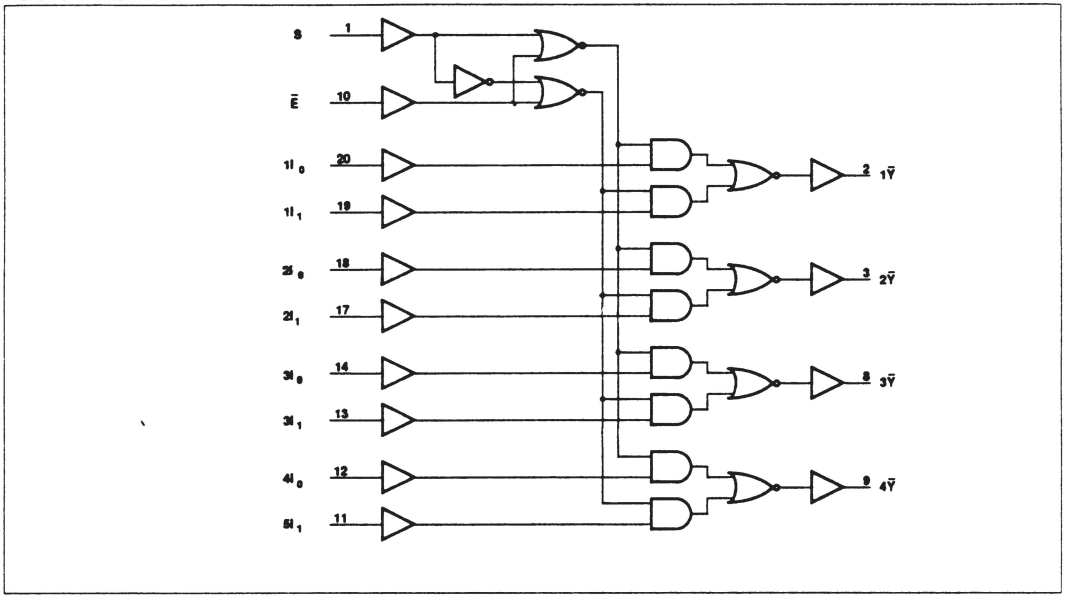
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	nI_0 - nI_0	Data inputs
19, 17, 13, 11	nI_1 - nI_1	Data inputs
2, 3, 8, 9	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
10	$\overline{E}$	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	nI_0	nI_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11158			74ACT11158			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]		3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0			ns/V
		Select and Enable	0		5	0			
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11158				74ACT11158				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11158					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	2	1.5 1.5	5.3 5.4	7.3 7.7	1.5 1.5	7.9 8.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $n\overline{Y}$	1	1.5 1.5	5.3 5.8	7.2 7.8	1.5 1.5	7.9 8.7	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	2	1.5 1.5	6.0 6.2	8.1 8.5	1.5 1.5	8.9 9.4	ns

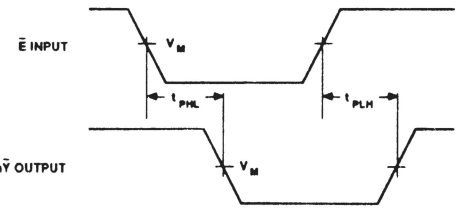
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11158					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	2	1.5 1.5	3.8 4.0	5.4 5.6	1.5 1.5	5.7 6.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $n\overline{Y}$	1	1.5 1.5	3.9 4.3	5.4 5.8	1.5 1.5	5.9 6.4	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	2	1.5 1.5	4.3 4.5	6.1 6.1	1.5 1.5	6.7 6.9	ns

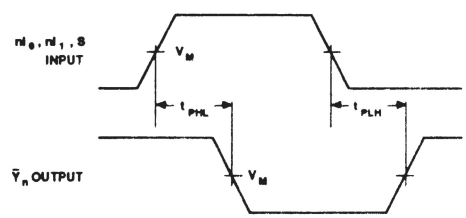
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11158					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $n\overline{Y}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	2	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Enable Input ($\overline{E}$) to Output ($n\overline{Y}$) Propagation Delays



Waveform 2. Waveforms Showing the Data Inputs (nI_0, nI_1) and Select Input (S) to Output ($n\overline{Y}$) Propagation Delays

74AC/ACT11160

Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

Preliminary Specification

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11160 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11160 4-bit synchronous presettable decade counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF; V_{CC} = 5V	6.4		ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	49		pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5		pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V	175		MHz

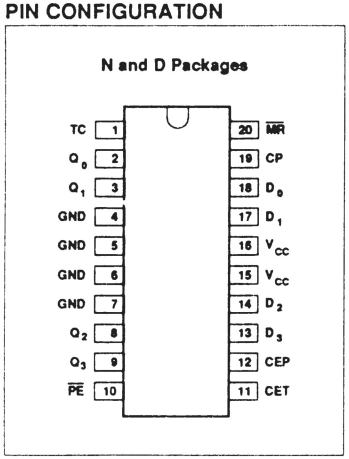
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

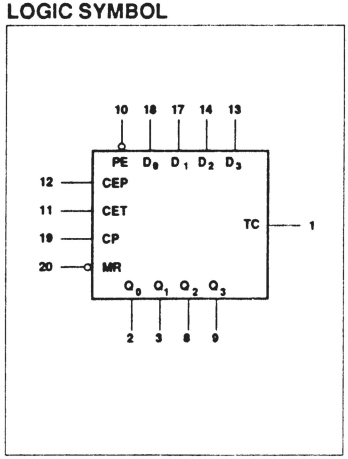
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11160N 74ACT11160N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11160D 74ACT11160D

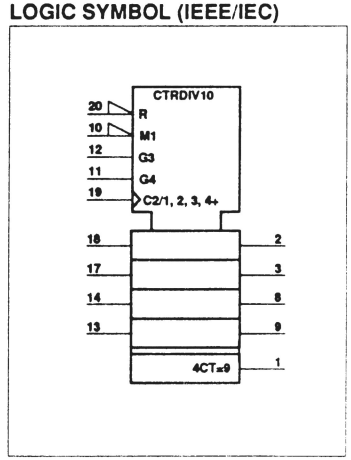
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous Presettable Synchronous BCD Decade Counter; Asynchronous Reset

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels, regardless of the levels at CP, $\overline{PE}$, CET, and CEP inputs (thus providing an asynchronous clear function).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{MR}$	Asynchronous master reset (active Low)
19	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
18, 17, 14, 13	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

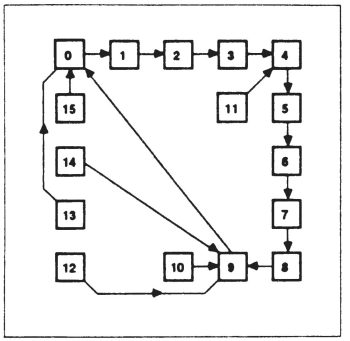
OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load[1]	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	
Count[1]	H	↑	h	h	h	X	count	
Hold (do nothing)[1]	H	X	l	X	h	X	q_n	
	H	X	X	l	h	X	q_n	L

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition

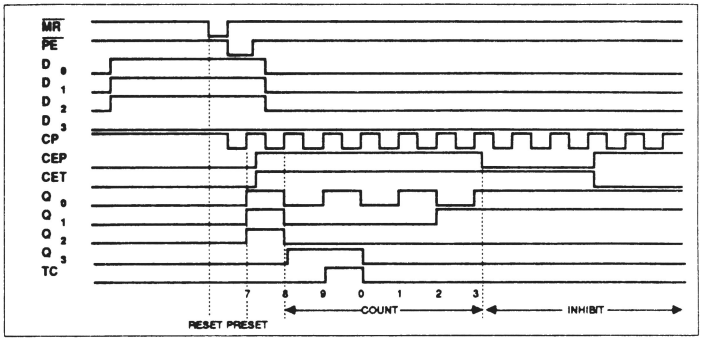
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HLLH).

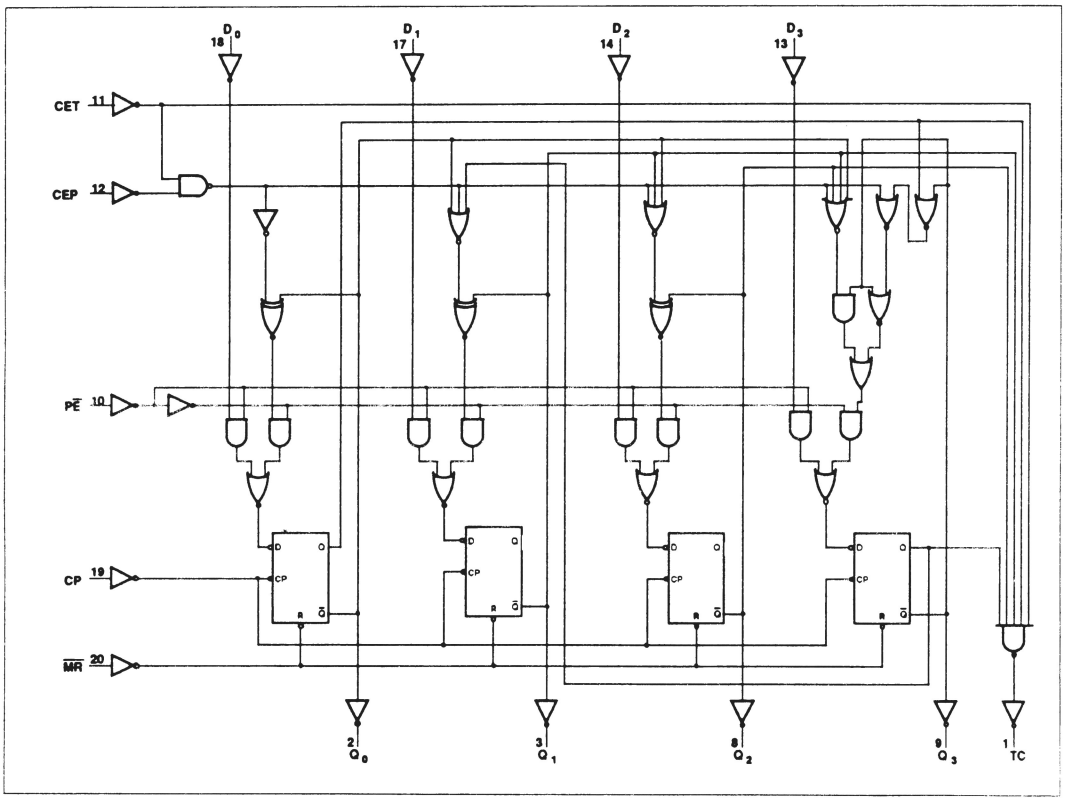
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11160			74ACT11160			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11160				74ACT11160				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11160					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	8.4 9.0	11.4 12.1	1.5 1.5	12.5 13.6	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	8.2 8.5	10.9 11.4	1.5 1.5	12.1 12.7	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	10.6 11.2	13.7 14.1	1.5 1.5	15.2 16.1	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5	5.9 6.1	7.9 8.2	1.5 1.5	8.6 8.9	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	9.2	12.1	1.5	13.4	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5	11.7	14.4	1.5	16.3	ns
t_S	Setup time, High or Low D_n to CP	4	4.0			4.5		ns
t_H	Hold time, High or Low D_n to CP	4	0.0			0.5		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	5.5			6.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	0.0			0.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	5.0			5.5		ns
t_H	Hold time, High or Low CEP or CET to CP	5	0.0			0.0		ns
t_W	Clock pulse width (load) High or Low	1	4.6			5.6		ns
t_W	Clock pulse width (count) High or Low	1	4.6			5.6		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.6			5.6		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	5.5			6.0		ns

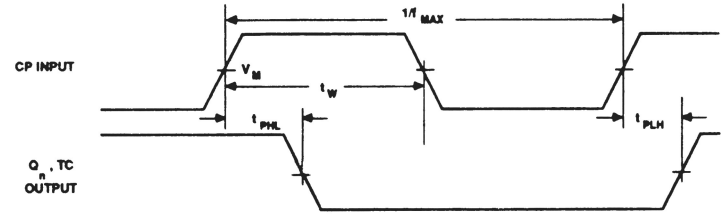
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11160					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	150	175		130		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	6.1 6.6	8.3 8.9	1.5 1.5	9.0 9.9	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	6.0 6.4	8.0 8.4	1.5 1.5	8.8 9.3	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	7.4 8.4	9.4 10.4	1.5 1.5	10.3 11.9	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5	4.3 4.9	5.8 6.4	1.5 1.5	6.3 7.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	6.8	8.8	1.5	10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5	8.7	10.8	1.5	12.0	ns
t_S	Setup time, High or Low D_n to CP	4	3.0			3.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	4.0			4.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	0.5			0.5		ns
t_S	Setup time, High or Low CEP or CET to CP	5	3.5			4.0		ns
t_H	Hold time, High or Low CEP or CET to CP	5	0.5			0.5		ns
t_W	Clock pulse width (load) High or Low	1	3.3			3.9		ns
t_W	Clock pulse width (count) High or Low	1	3.3			3.9		ns
t_W	$\overline{MR}$ pulse width, Low	2	3.3			3.7		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	4.0			4.5		ns

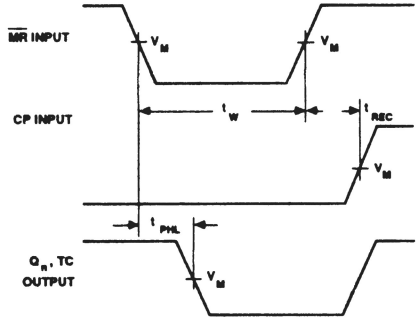
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f = 3ns$; $C_L = 50pF$

SYMBOL	PARAMETER	WAVEFORM	74ACT11160					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1						MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5			1.5 1.5		ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5			1.5		ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5			1.5		ns
t_S	Setup time, High or Low D_n to CP	4						ns
t_H	Hold time, High or Low D_n to CP	4						ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4						ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4						ns
t_S	Setup time, High or Low CEP or CET to CP	5						ns
t_H	Hold time, High or Low CEP or CET to CP	5						ns
t_W	Clock pulse width (load) High or Low	1						ns
t_W	Clock pulse width (count) High or Low	1						ns
t_W	$\overline{MR}$ pulse width, Low	2						ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2						ns

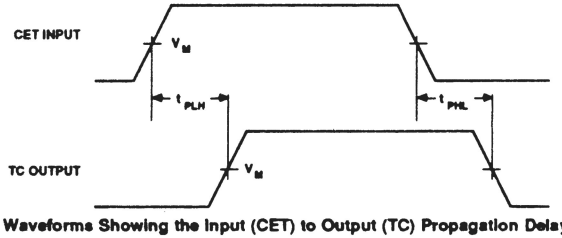
AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width

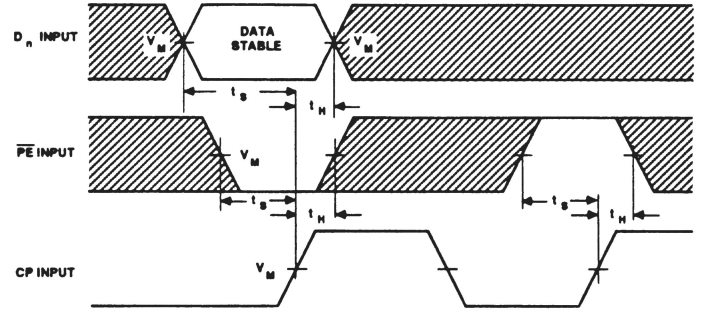


Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Qn, TC) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

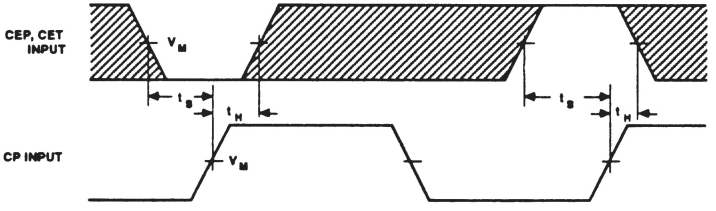


Waveform 3. Waveforms Showing the Input (CET) to Output (TC) Propagation Delays

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 4. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n) and Parallel Enable Input $\overline{PE}$



Waveform 5. Waveforms Showing CEP and CET Set-up and Hold Times

74AC/ACT11162

Synchronous Presettable BCD Decade Counter; Synchronous Reset

Preliminary Specification

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Synchronous reset
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{cc} and ground configuration to minimize high-speed switching noise
- I_{cc} category: MSI

DESCRIPTION

The 74AC/ACT11162 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11162 4-bit synchronous presettable decade counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF; V_{CC} = 5V	6.4		ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	66		pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5		pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V	175		MHz

Note:

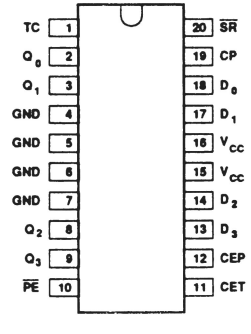
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

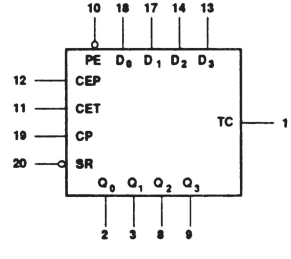
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11162N 74ACT11162N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11162D 74ACT11162D

PIN CONFIGURATION

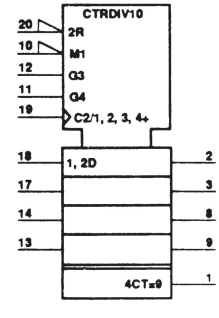
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous Presettable BCD Decade Counter; Synchronous Reset

74AC/ACT11162

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels after the next positive-going transition on the clock (CP) input. This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{SR}$	Synchronous reset (active Low)
19	CP	Clock input (Low-to-High edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
18, 17, 14, 13	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load[1]	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	
Count[1]	h	↑	h	h	h	X	count	
Hold (do nothing)[1]	h	X	l	X	h	X	q_n	
	h	X	X	l	h	X	q_n	L

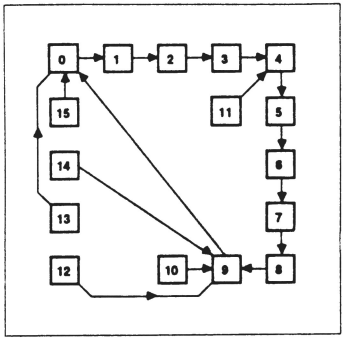
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HLLH).

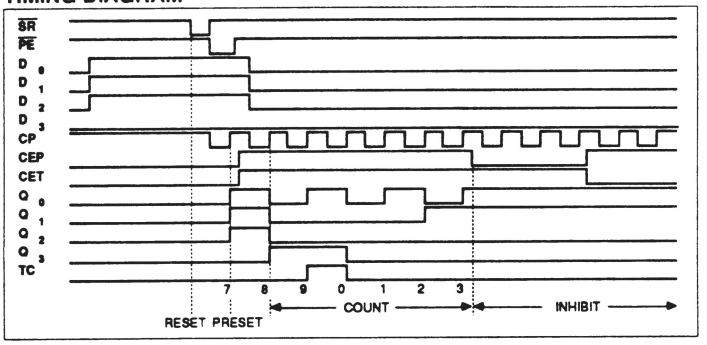
Synchronous Presettable BCD Decade Counter; Synchronous Reset

74AC/ACT11162

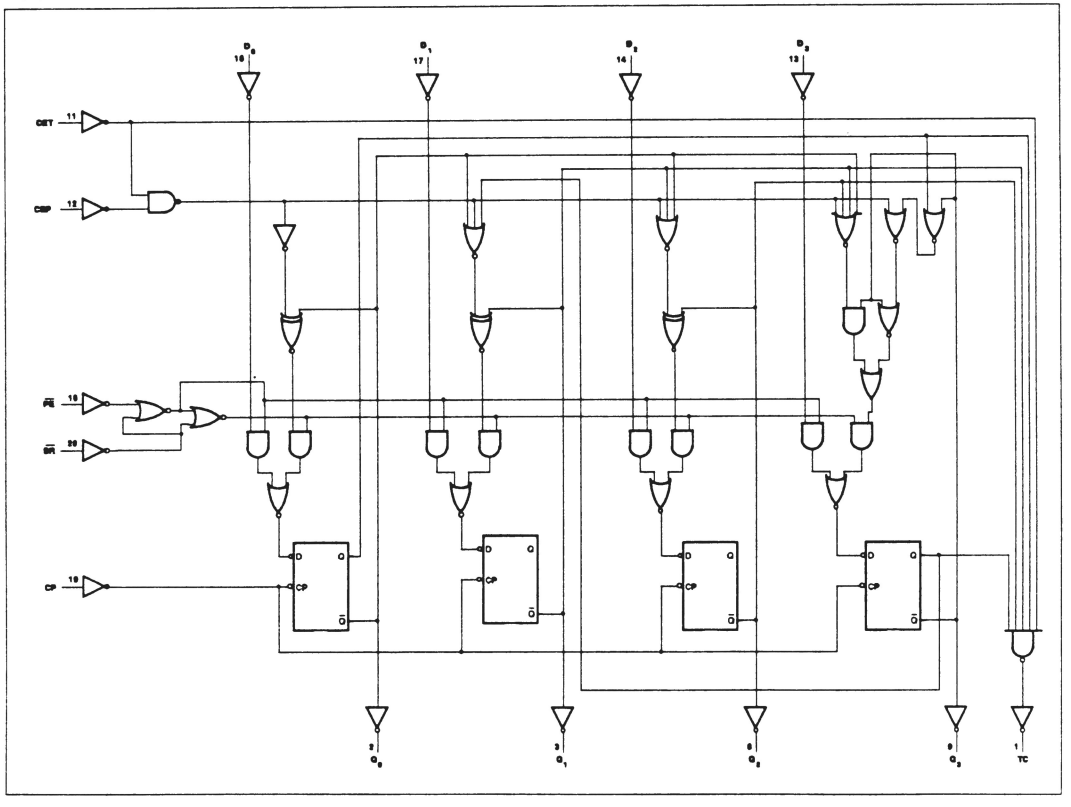
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11162			74ACT11162			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11162				74ACT11162				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11162					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	8.4 9.0	11.4 12.1	1.5 1.5	12.5 13.6	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	8.2 8.5	10.9 11.4	1.5 1.5	12.1 12.7	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	10.6 11.2	13.7 14.1	1.5 1.5	15.2 16.1	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.5 1.5	5.9 6.1	7.9 8.2	1.5 1.5	8.6 8.9	ns
t_S	Setup time, High or Low D_n to CP	3	4.0			4.5		ns
t_H	Hold time, High or Low D_n to CP	3	0.0			0.5		ns
t_S	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	3	5.5			6.0		ns
t_H	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	3	0.0			0.0		ns
t_S	Setup time, High or Low CEP or CET to CP	4	5.0			5.5		ns
t_H	Hold time, High or Low CEP or CET to CP	4	0.0			0.0		ns
t_W	Clock pulse width (load) High or Low	1	4.6			5.6		ns
t_W	Clock pulse width (count) High or Low	1	4.6			5.6		ns

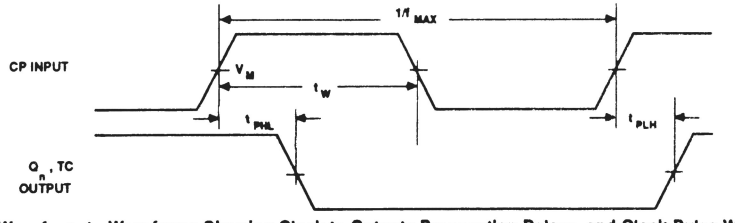
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11162					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	150	175		130		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	6.1 6.6	8.3 8.9	1.5 1.5	9.0 9.9	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	6.0 6.4	8.0 8.4	1.5 1.5	8.8 9.3	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	7.4 8.4	9.4 10.4	1.5 1.5	10.3 11.9	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.5 1.5	4.3 4.9	5.8 6.4	1.5 1.5	6.3 7.2	ns
t_S	Setup time, High or Low D_n to CP	3	3.0			3.5		ns
t_H	Hold time, High or Low D_n to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	3	0.5			0.5		ns
t_S	Setup time, High or Low CEP or CET to CP	4	3.5			4.0		ns
t_H	Hold time, High or Low CEP or CET to CP	4	0.5			0.5		ns
t_W	Clock pulse width (load) High or Low	1	3.3			3.9		ns
t_W	Clock pulse width (count) High or Low	1	3.3			3.9		ns

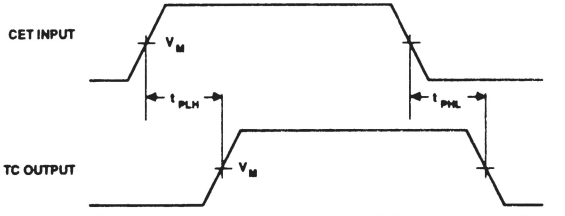
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11162					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1						MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.5 1.5			1.5 1.5		ns
t_S	Setup time, High or Low D_n to CP	3						ns
t_H	Hold time, High or Low D_n to CP	3						ns
t_S	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	3						ns
t_H	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	3						ns
t_S	Setup time, High or Low CEP or CET to CP	4						ns
t_H	Hold time, High or Low CEP or CET to CP	4						ns
t_W	Clock pulse width (load) High or Low	1						ns
t_W	Clock pulse width (count) High or Low	1						ns

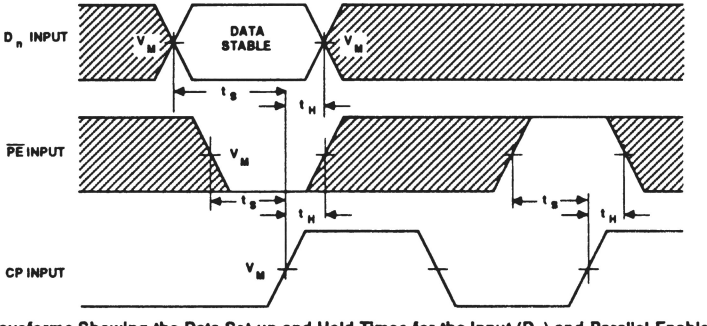
AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



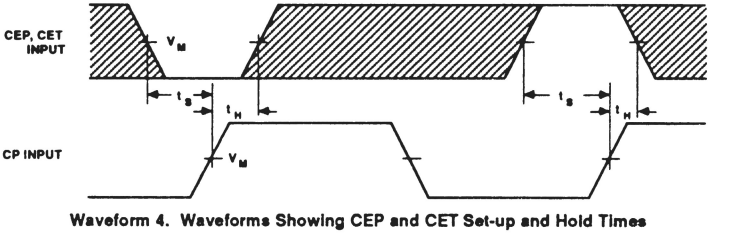
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays, and Clock Pulse Width



Waveform 2. Waveforms Showing the Input (CET) to Output (TC) Propagation Delays



Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n) and Parallel Enable Input $\overline{PE}$



Waveform 4. Waveforms Showing CEP and CET Set-up and Hold Times

74AC/ACT11175

Quad D-Type Flip-Flop w/Reset; Positive-Edge Trigger

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11175 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11175 provides four D-type flip-flops with independent Data inputs, shared Clock and Master Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Master Reset ($\overline{MR}$) is an asynchronous active-Low input and operates independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering is threshold voltage dependent. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
		T_A = 25°C; GND = 0V	AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	C_L = 50pF; V_{CC} = 5V	6.3	7.3	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	47	42	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V	135	120	MHz

Note:

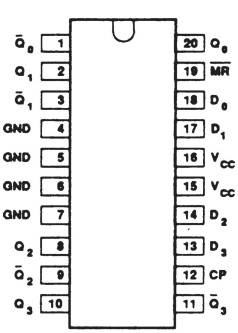
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

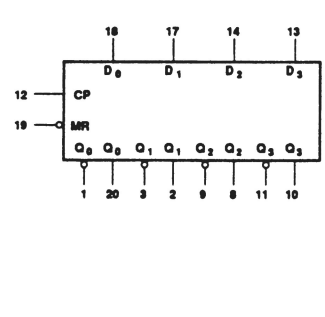
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11175N 74ACT11175N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11175D 74ACT11175D

PIN CONFIGURATION

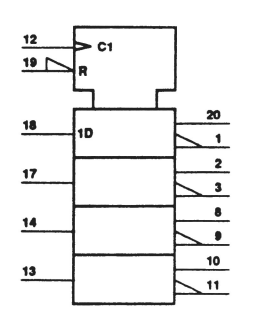
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

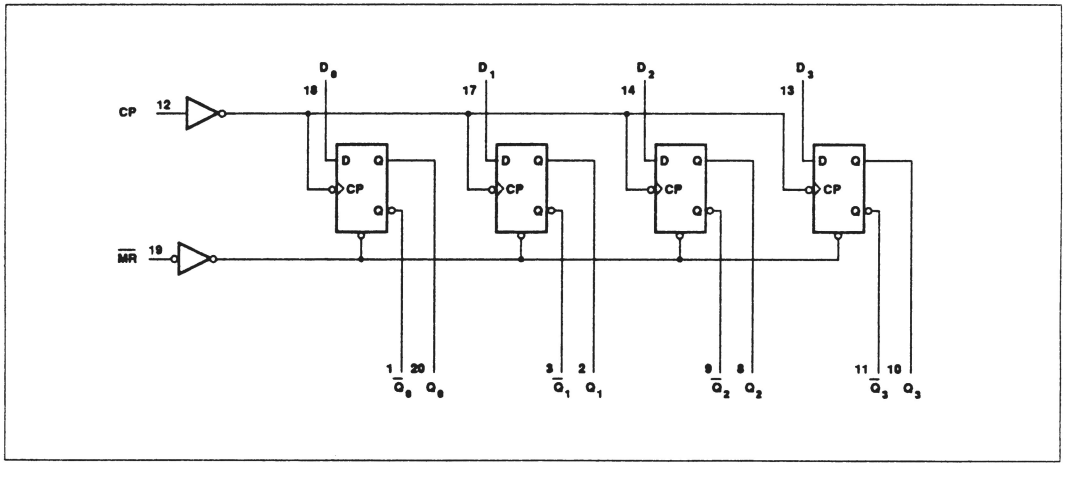
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17, 14, 13	D_0 - D_3	Data inputs
20, 2, 8, 10	Q_0 - Q_3	Data outputs
1, 3, 9, 11	$\overline{Q}_0$ - $\overline{Q}_3$	Data outputs (complements of Q_n outputs)
19	$\overline{MR}$	Master reset input (active Low)
12	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Asynchronous reset	L	X	X	L	H
Load "1" (set)	H	↑	h	H	L
Load "0" (reset)	H	↑	l	L	H

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11175			74ACT11175			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11175				74ACT11175				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	115		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	7.8 10.8	10.0 13.7	1.5 1.5	10.9 14.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	7.9 11.4	9.8 13.7	1.5 1.5	10.6 14.6	ns
t_S	Setup time, High or Low D_n to CP	1	8.0			8.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

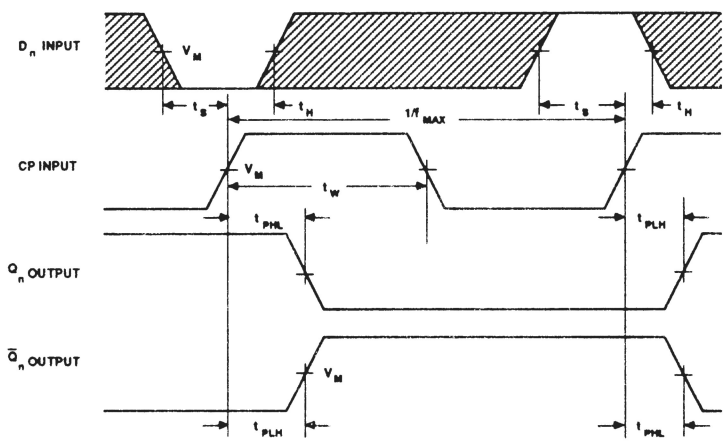
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	135		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	5.4 7.2	7.2 9.8	1.5 1.5	7.8 10.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	5.4 8.1	7.0 9.8	1.5 1.5	7.5 10.7	ns
t_S	Setup time, High or Low D_n to CP	1	5.5			5.5		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	4.5			4.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

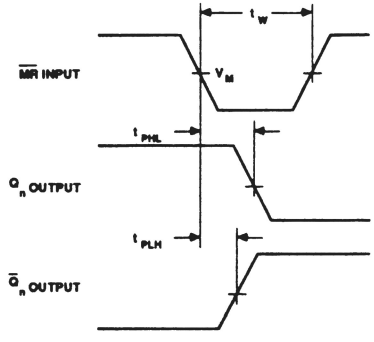
SYMBOL	PARAMETER	WAVEFORM	74ACT11175					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	120		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	6.1 8.4	7.8 10.6	1.5 1.5	8.3 11.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	6.9 9.5	8.4 11.6	1.5 1.5	8.9 12.5	ns
t_S	Setup time, High or Low D_n to CP	1	5.5			5.5		ns
t_H	Hold time, High or Low CP to D_n	1	1.0			1.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.5			1.5		ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V

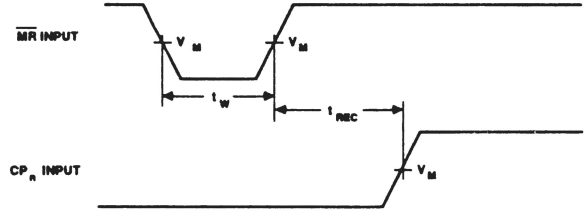


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 2. Waveforms Showing Reset to Output Delay and Reset Pulse Width



Waveform 3. Waveforms Showing Recovery Time

74AC/ACT11190

Asynchronous Presettable Synchronous Decade Up/Down Counter w/Single Clock

Preliminary Specification

FEATURES

- **High-speed—___MHz typical f_{max}**
- **Synchronous, reversible counting**
- **Positive edge-triggered clock**
- **BCD/decade**
- **Asynchronous Parallel Load capability**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{cc} and ground configuration to minimize high-speed switching noise**
- **I_{cc} category: MSI**

DESCRIPTION

The 74AC/ACT11190 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF; V_{CC} = 5V			ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF			pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}			pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V			MHz

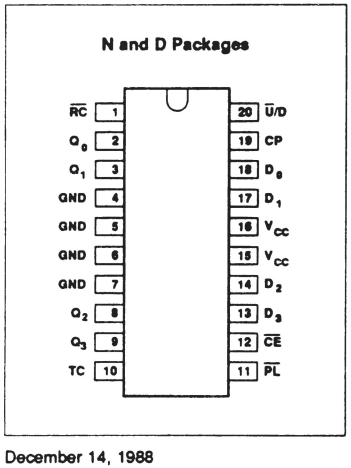
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

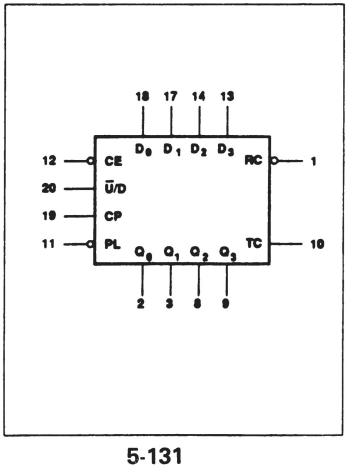
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11190N 74ACT11190N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11190D 74ACT11190D

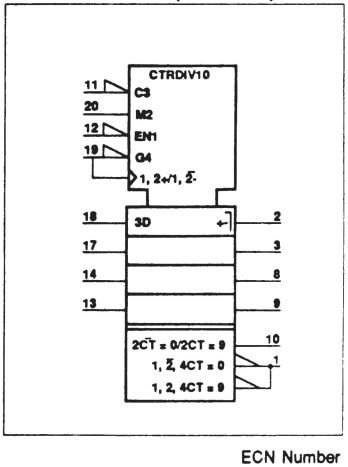
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Asynchronous Presettable Synchronous Decade Up/Down Counter w/Single Clock

Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

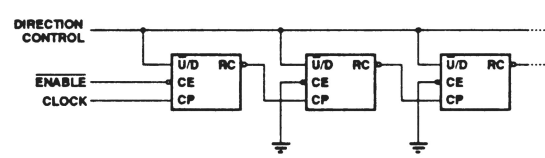
Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "9" in the Count-up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the Clock Pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. The 74AC/ACT11190 simplifies the design of multistage counters, as indicated in Figures 1a and 1b.

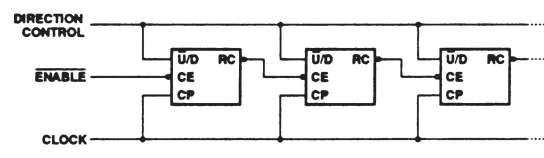
In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the Clock input source has limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

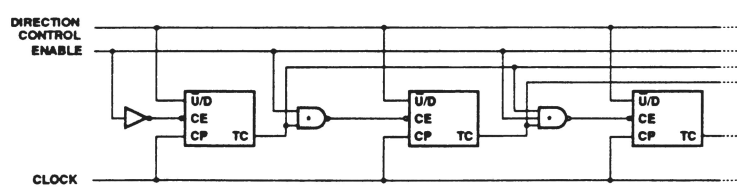
In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.



a. N-Stage Counter Using Ripple Clock



b. Synchronous N-Stage Counter with Common Clock Using Ripple Clock



c. Synchronous N-Stage Counter with Common Clock and Parallel Gated Terminal Count

Figure 1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{U}/D$	Up/down count control input
12	$\overline{CE}$	Count enable input (active-Low)
18, 17, 14, 13	$D_0 - D_3$	Data inputs
19	CP	Clock pulse input (active rising edge)
11	$\overline{PL}$	Asynchronous load input (active-Low)
2, 3, 8, 9	$Q_0 - Q_3$	Counter outputs
1	$\overline{RC}$	Ripple clock output (active-Low)
10	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold (do nothing)	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

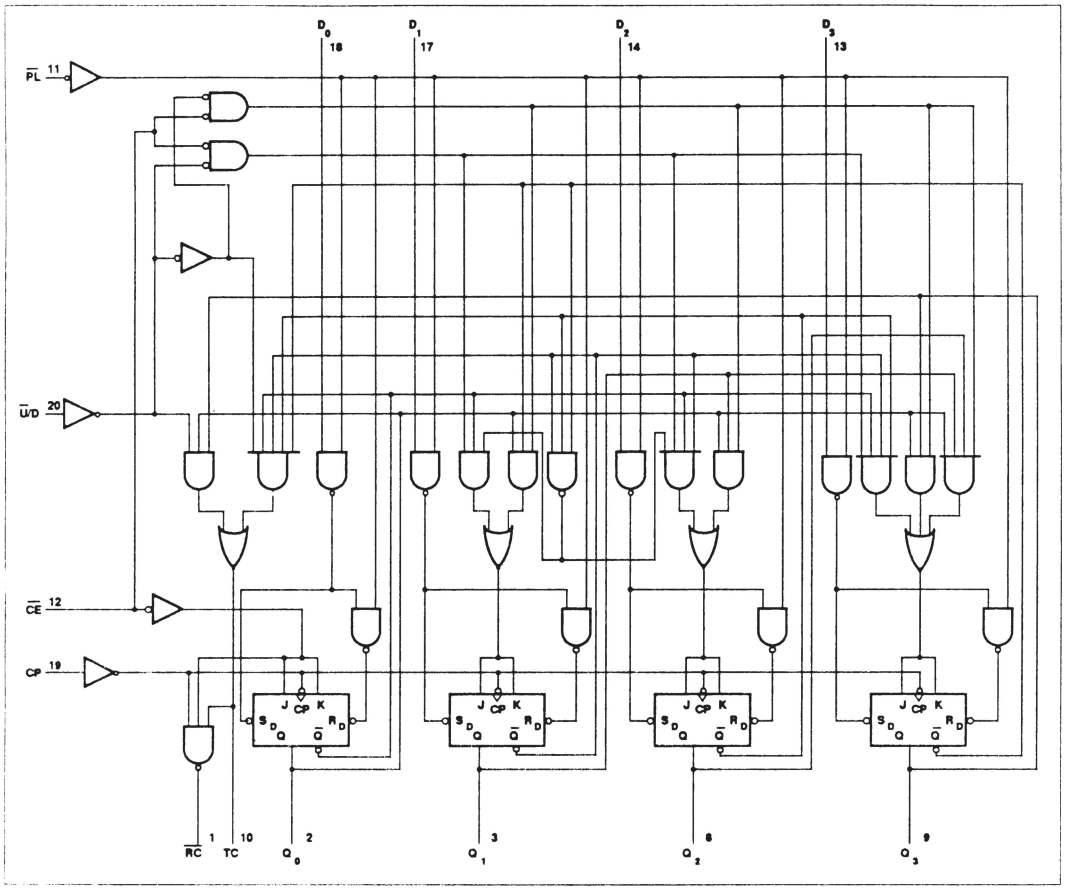
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊓	H	X	X	H	H	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	H	⊓

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊓ = Low pulse

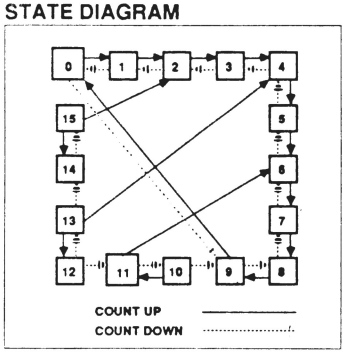
Asynchronous Presettable Synchronous Decade Up/Down Counter w/Single Clock

74AC/ACT11190

LOGIC DIAGRAM



STATE DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11190			74ACT11190			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11190				74ACT11190				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER		WAVEFORM	74AC11190					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1						MHz
		CP to $\overline{RC}$							MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n)		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3						ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5						ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6						ns
$t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6						ns
$t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6						ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6						ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5						ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1						ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5						ns

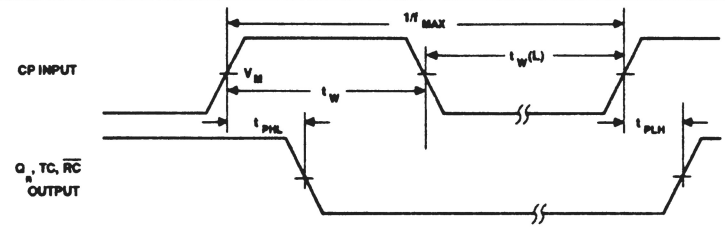
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f = 3ns$; $C_L = 50pF$

SYMBOL	PARAMETER		WAVEFORM	74AC11190					UNIT
				$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1						MHz
		CP to $\overline{RC}$							MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n)		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3						ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5						ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6						ns
$t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6						ns
$t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6						ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6						ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5						ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1						ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5						ns

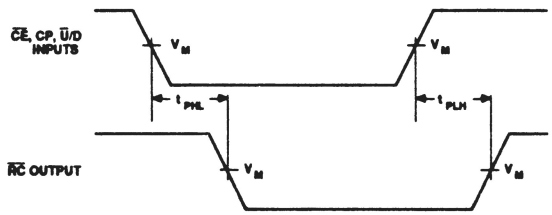
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER		WAVEFORM	74ACT11190					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1						MHz
		CP to $\overline{RC}$							MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n)		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3						ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5						ns
$t_S(H)$ $t_S(L)$	Setup time High or Low D_n to $\overline{PL}$		6						ns
$t_h(H)$ $t_h(L)$	Hold time High or Low D_n to $\overline{PL}$		6						ns
$t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6						ns
$t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6						ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6						ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5						ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1						ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5						ns

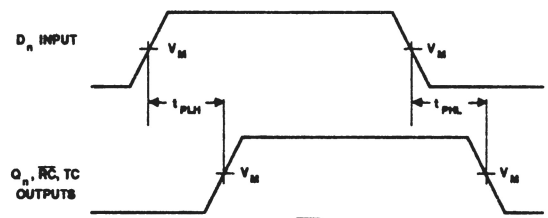
AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



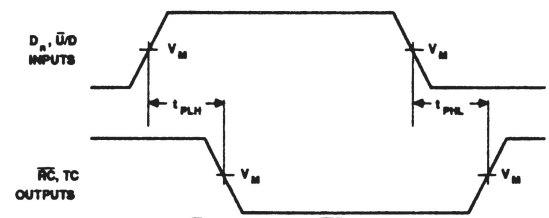
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Clock, Count Enable, or U/D to Ripple Clock Output Propagation Delay

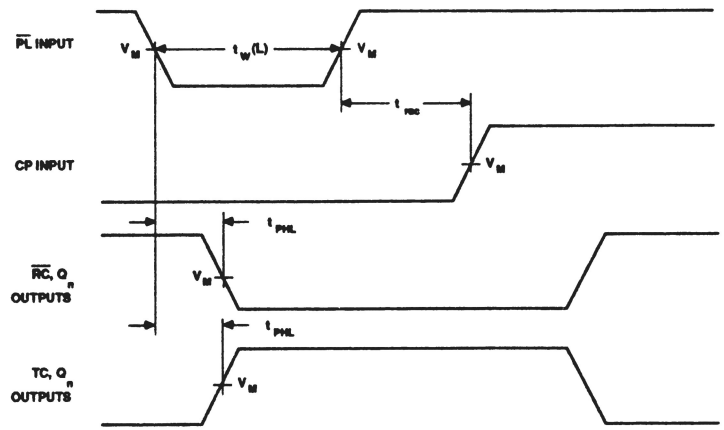


Waveform 3. Waveforms Showing the Input (D_n) to Output (Q_n, $\overline{RC}$, TC) Propagation Delays, Non-Inverting Path

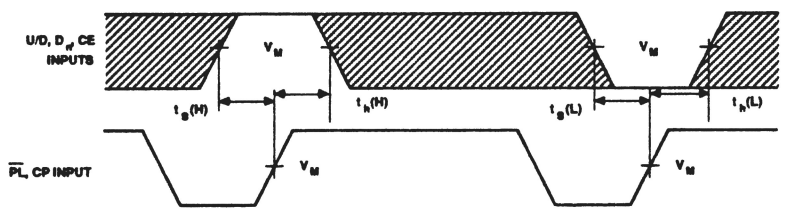


Waveform 4. Waveforms Showing the Input (D_n, U/D) to Output ($\overline{RC}$, TC) Propagation Delays, Inverting Path

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 5. Waveforms Showing the Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



Waveform 6. Waveforms Showing Setup Time and Hold Time for D_n to $\overline{PL}$, U/D to CP and $\overline{CE}$ to CP

74AC/ACT11191

Asynchronous Presettable Synchronous 4-Bit Binary Up/ Down Counter w/Single Clock

Preliminary Specification

FEATURES

- High-speed—___MHz typical f_{max}
- Synchronous, reversible counting
- Positive edge-triggered clock
- 4-bit binary
- Asynchronous Parallel Load capability
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{cc} and ground configuration to minimize high-speed switching noise
- I_{cc} category: MSI

DESCRIPTION

The 74AC/ACT11191 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11191 is an asynchronously presettable up/down 4-bit binary counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF; V_{CC} = 5V			ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF			pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}			pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V			MHz

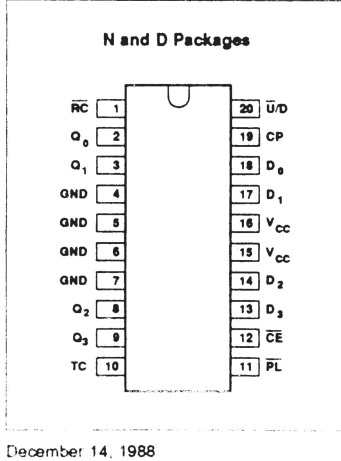
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

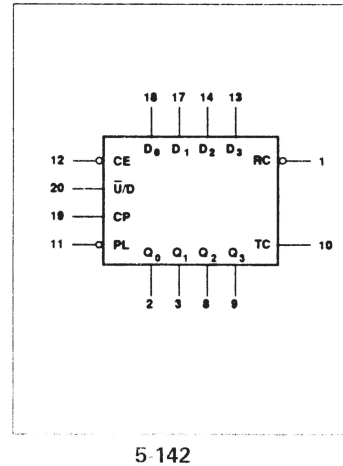
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11191N 74ACT11191N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11191D 74ACT11191D

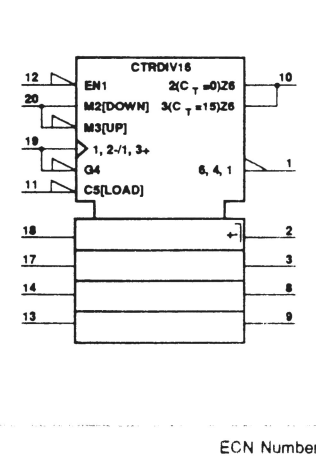
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Single Clock

74AC/ACT11191

Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

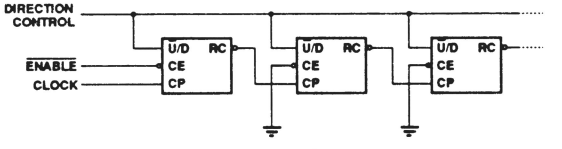
Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "15" in the Count-up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the Clock Pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. The 74AC/ACT11191 simplifies the design of multistage counters, as indicated in Figures 1a and 1b.

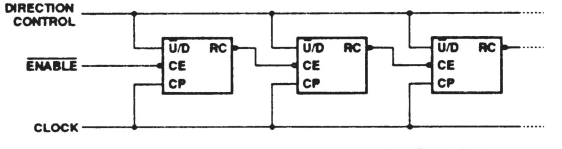
In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the Clock input source has limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

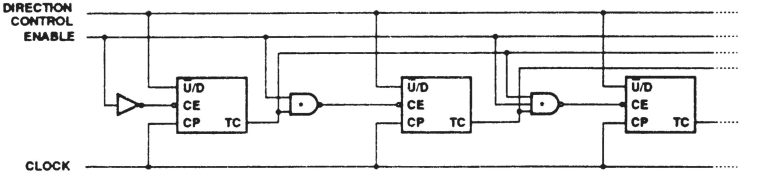
In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.



a. N-Stage Counter Using Ripple Clock



b. Synchronous N-Stage Counter with Common Clock Using Ripple Clock



c. Synchronous N-Stage Counter with Common Clock and Parallel Gated Terminal Count

Figure 1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{U}/D$	Up/down count control input
12	$\overline{CE}$	Count enable input (active-Low)
18, 17, 14, 13	D_0 - D_3	Data inputs
19	CP	Clock pulse input (active rising edge)
11	$\overline{PL}$	Asynchronous load input (active-Low)
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
1	$\overline{RC}$	Ripple clock output (active-Low)
10	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

MODE SELECT — FUNCTION TABLE

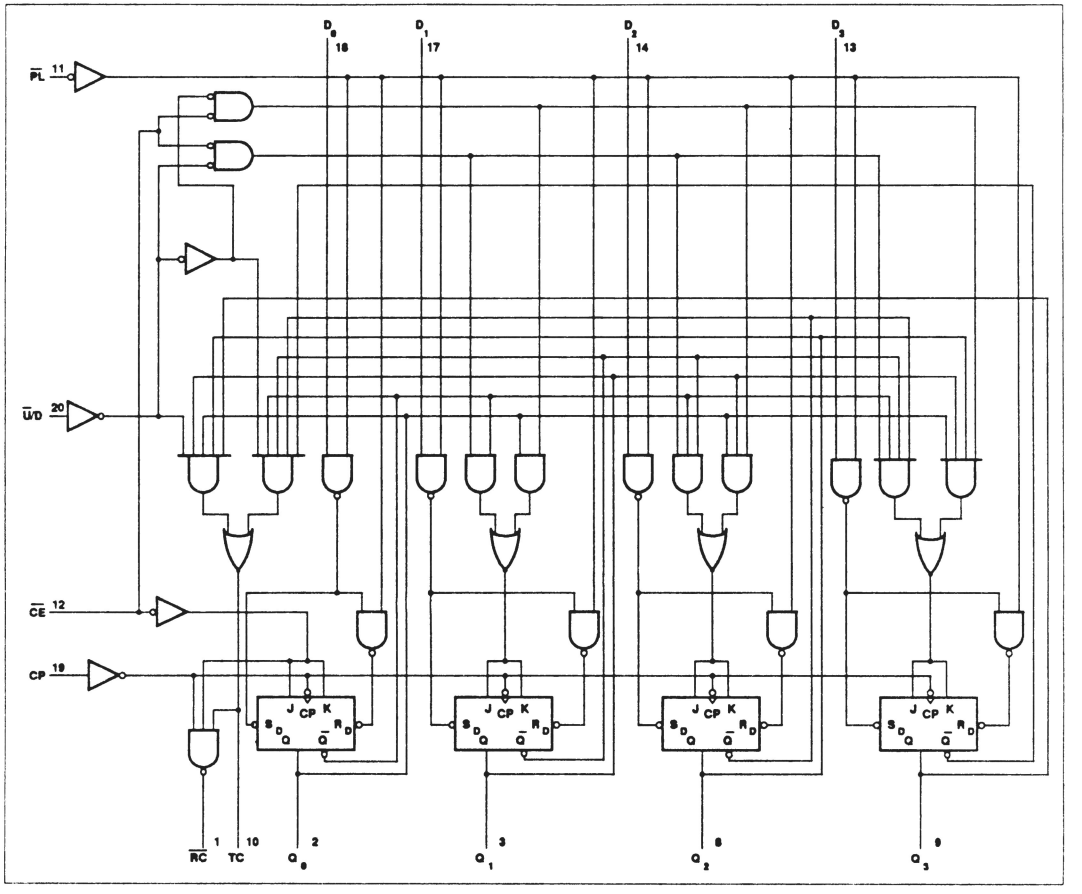
OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold (do nothing)	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

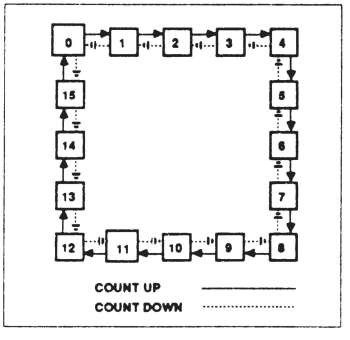
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	h	H	H	H	H	H
L	L	⊓	H	H	H	H	H	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	H	⊓

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
↑ = Low-to-High clock transition
↓ = High-to-Low Trickle Clock transition
⊓ = Low pulse

LOGIC DIAGRAM



STATE DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11191			74ACT11191			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11191				74ACT11191				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER		WAVEFORM	74AC11191					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1						MHz
		CP to $\overline{RC}$							MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n)		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to $\overline{RC}$		2						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to TC		4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3						ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5						ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6						ns
$t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6						ns
$t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6						ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}/D$ to CP		6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}/D$ to CP		6						ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5						ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1						ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5						ns

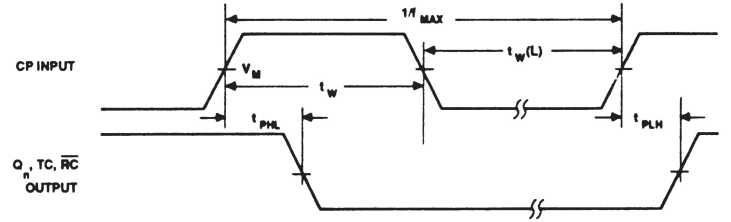
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER		WAVEFORM	74AC11191					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1						MHz
		CP to $\overline{RC}$							MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n)		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3						ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5						ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_n to $\overline{PL}$		6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$		6						ns
$t_S(L)$	Setup time, High or Low $\overline{CE}$ to CP		6						ns
$t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		6						ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{U}$/D to CP		6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP		6						ns
$t_w(L)$	$\overline{PL}$ pulse width, Low		5						ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low		1						ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5						ns

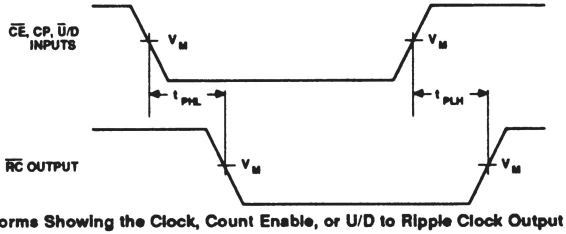
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER		WAVEFORM	74ACT11191					UNIT
				T_A = +25°C			T_A = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1						MHz
		CP to $\overline{RC}$							MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n)		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3						ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5						ns
t_S(H) t_S(L)	Setup time, High or Low D_n to $\overline{PL}$		6						ns
t_h(H) t_h(L)	Hold time, High or Low D_n to $\overline{PL}$		6						ns
t_S(L)	Setup time, High or Low $\overline{CE}$ to CP		6						ns
t_h(L)	Hold time, High or Low $\overline{CE}$ to CP		6						ns
t_S(H) t_S(L)	Setup time, High or Low $\overline{U}$/D to CP		6						ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{U}$/D to CP		6						ns
t_w(L)	$\overline{PL}$ pulse width, Low		5						ns
t_w(H) t_w(L)	CP pulse width, High or Low		1						ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5						ns

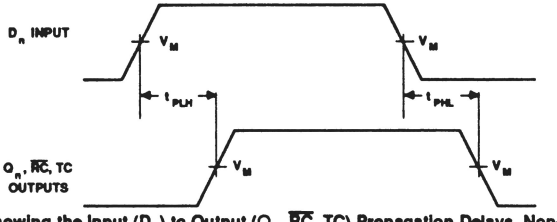
AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



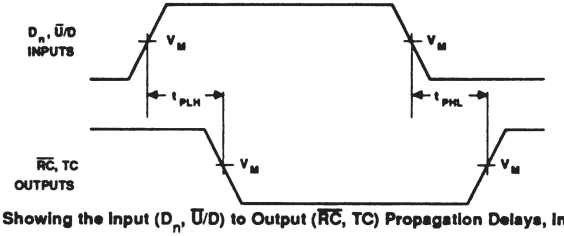
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Clock, Count Enable, or U/D to Ripple Clock Output Propagation Delay

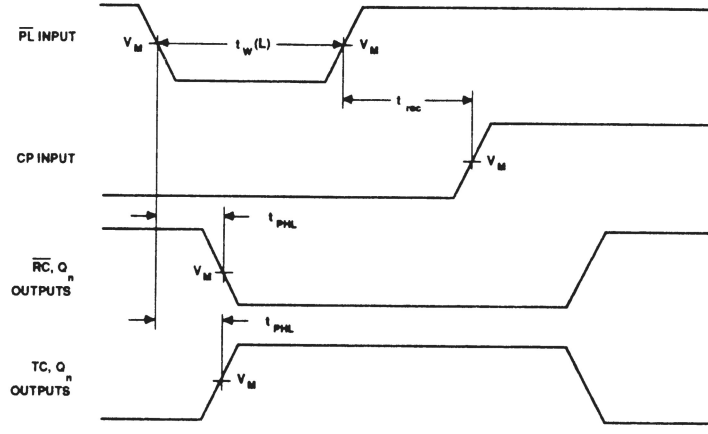


Waveform 3. Waveforms Showing the Input (D_n) to Output (Q_n, $\overline{RC}$, TC) Propagation Delays, Non-Inverting Path

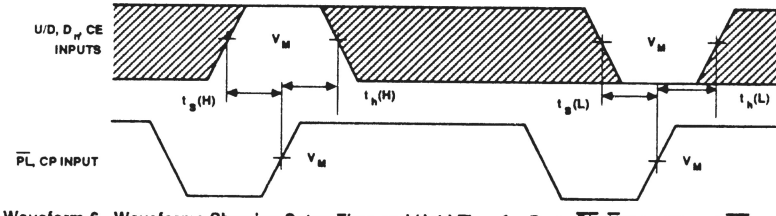


Waveform 4. Waveforms Showing the Input (D_n, $\overline{U}$/D) to Output ($\overline{RC}$, TC) Propagation Delays, Inverting Path

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 5. Waveforms Showing the Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



Waveform 6. Waveforms Showing Setup Time and Hold Time for D_n to $\overline{PL}$, $\overline{U}$/D to CP and $\overline{CE}$ to CP

74AC/ACT11194

4-Bit Bidirectional Universal Shift Register

Preliminary Specification

FEATURES

- **Shift left and shift right capability**
- **Synchronous Parallel and Serial data transfers**
- **Easily expanded for both Serial and Parallel operation**
- **Asynchronous reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11194 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11194 4-bit Bidirectional Universal Shift Register is fully synchronous, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n ($\overline{MR}$ = High)	C_L = 50pF; V_{CC} = 5V	4.8	5.8	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	66	69	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V	150	130	MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:

   f_I = input frequency in MHz, C_L = output load capacitance in pF,

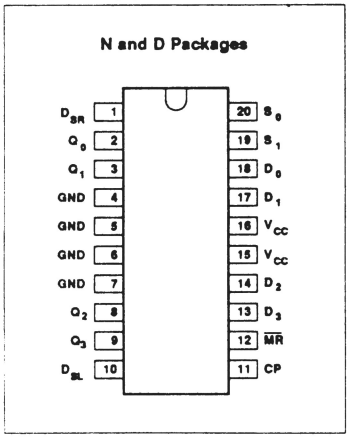
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,

   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

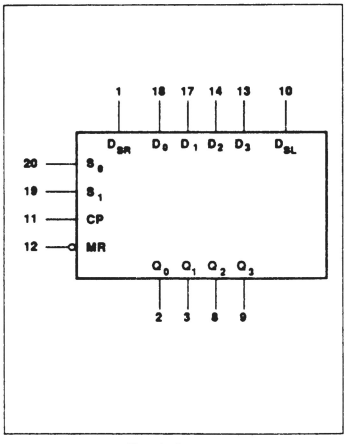
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11194N 74ACT11194N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11194D 74ACT11194D

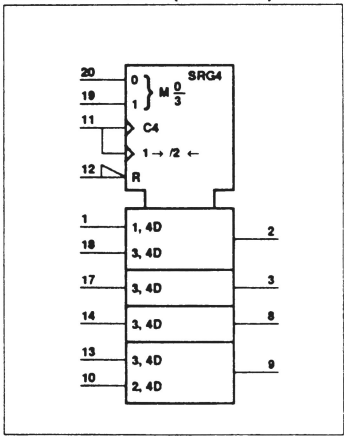
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The 74AC/ACT11194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Function Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_0 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data input (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode select and Data inputs on the 74AC/ACT11194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. Signals on the Select, Parallel Data (D_0 - D_3) and Serial Data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge are observed.

The four Parallel Data inputs (D_0 - D_3) are D-type inputs. Data appearing on D_0 - D_3 inputs when S_0 and S_1 are High is transferred to the Q_0 - Q_3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

PIN DESCRIPTION

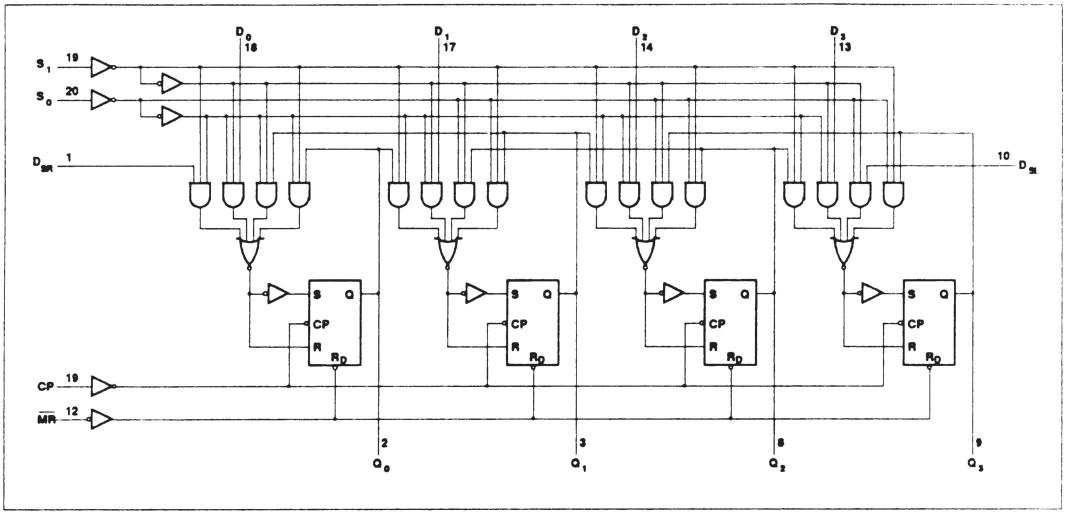
PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	$\overline{MR}$	Asynchronous master reset (active Low)
11	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
1	D_{SR}	Serial data input (shift right)
10	D_{SL}	Serial data input (shift left)
20, 19	S_0, S_1	Mode control inputs
2, 3, 8, 9	Q_0 - Q_3	Parallel outputs outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	↑	H	h	l	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	↑	H	l	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	↑	H	h	h	X	X	dn	d_0	d_1	d_2	d_3

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
d_n (q_n) = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11194			74ACT11194			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11194				74ACT11194				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	6.4 7.1	8.9 9.5	1.5 1.5	9.5 10.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	7.6	10.2	1.5	10.9	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	0.0			0.0		ns
t_S	Setup time, High or Low S_n to CP	3	5.5			5.5		ns
t_H	Hold time, High or Low CP to S_n	3	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	0.5			0.5		ns

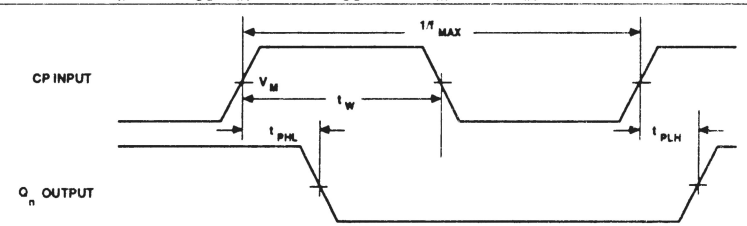
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	4.5 5.0	6.6 7.1	1.5 1.5	7.1 7.7	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	5.4	7.5	1.5	8.1	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	0.5			0.5		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	1.0			1.0		ns
t_S	Setup time, High or Low S_n to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to S_n	3	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	4.0			4.0		ns
t_W	Clock pulse width (count) High or Low	1	4.0			4.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f = 3ns$; $C_L = 50pF$

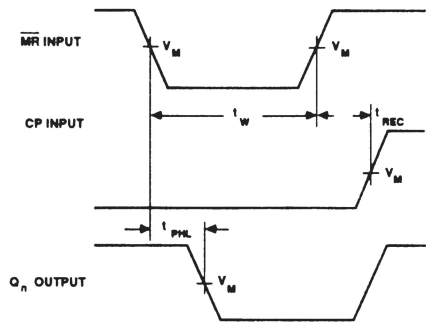
SYMBOL	PARAMETER	WAVEFORM	74ACT11194					UNIT
			$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	5.5 6.1	6.8 7.6	1.5 1.5	7.3 8.3	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	7.5	9.1	1.5	9.8	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	4.5			4.5		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	1.0			1.0		ns
t_S	Setup time, High or Low S_n to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low CP to S_n	3	2.0			2.0		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

AC WAVEFORMS AC : $V_M = 50\% V_{CC}$, $V_{IN} = GND$ to V_{CC}. ACT : $V_M = 1.5V$, $V_{IN} = GND$ to 3.0V

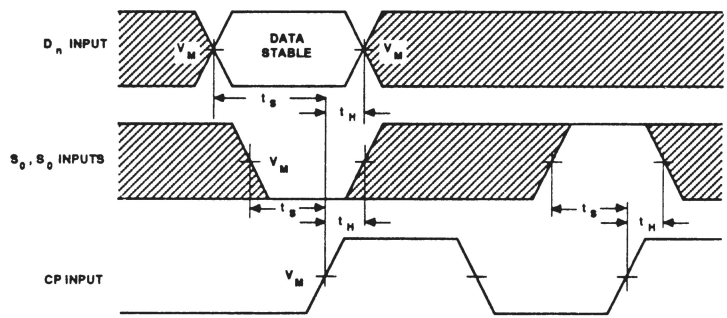


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Q_n) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time



Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n) and for S_0 and S_1 Inputs

74AC/ACT11238

3-to-8 Line Decoder/ Demultiplexer

Preliminary Specification

FEATURES

- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Non-inverting outputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11238 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11238 decoders accept three binary weighted inputs (A_0, A_1, A_2) and when enabled, provide eight mutually exclusive, active-High outputs (Y_0 - Y_7). The devices feature three enable inputs; two active-Low ($\overline{E}_1$, $\overline{E}_2$) and one active-High (E_3). Every output will be Low unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enable function allows easy parallel expansion of the devices to a 1-of-32 (5 lines to 32 lines) decoder with just four '11238's and one inverter.

The devices can be used as eight output demultiplexers by using one of the active-Low enable inputs as the data input and the remaining enable inputs as strobes.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF; V_{CC} = 5V	5.9	5.6	ns
C_{PD}	Power dissipation capacitance[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	55	57	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

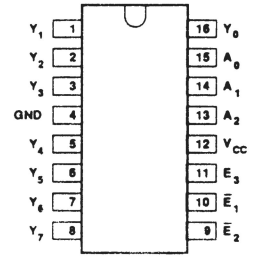
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

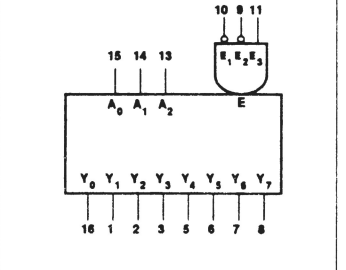
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11238N 74ACT11238N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11238D 74ACT11238D

PIN CONFIGURATION

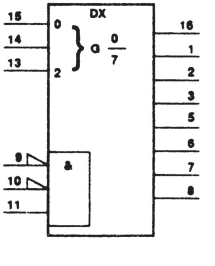
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



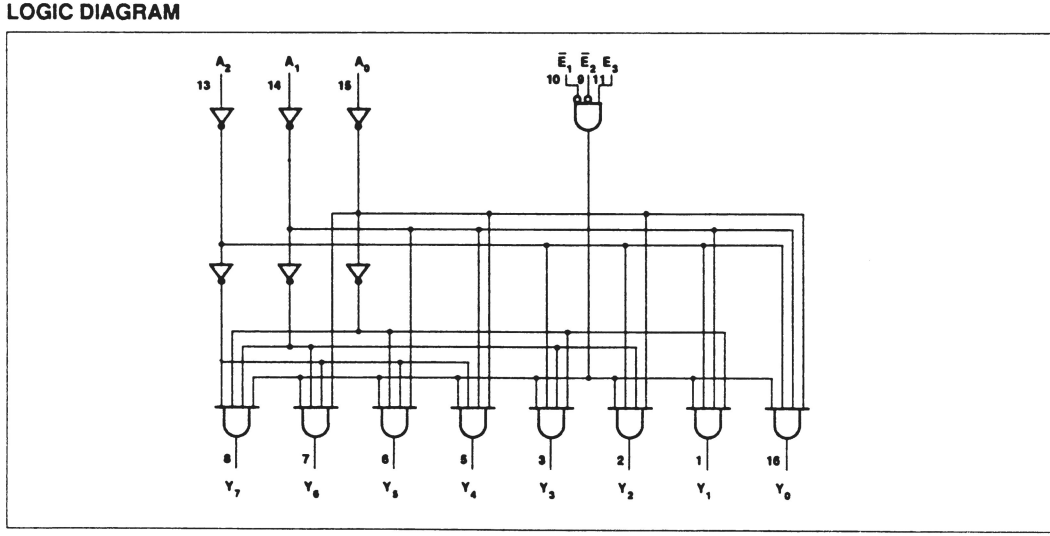
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14, 13	A_0 to A_2	Address inputs
10, 9	$\overline{E}_1$, $\overline{E}_2$	Enable inputs (active Low)
11	E_3	Enable input (active High)
16, 8, 7, 6, 5, 3, 2, 1	Y_0 to Y_7	Outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11238			74ACT11238			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11238				74ACT11238				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11238					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	8.5 9.6	10.6 11.9	1.5 1.5	11.7 13.3	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to Y_n	2	1.5 1.5	8.2 9.6	10.3 11.7	1.5 1.5	11.4 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y_n	2	1.5 1.5	9.1 10.7	11.2 12.9	1.5 1.5	12.5 14.5	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

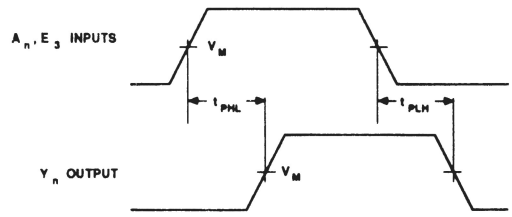
SYMBOL	PARAMETER	WAVEFORM	74AC11238					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	5.4 6.3	7.0 8.2	1.5 1.5	8.2 9.7	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to Y_n	2	1.5 1.5	5.2 6.5	6.7 8.2	1.5 1.5	7.9 9.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y_n	2	1.5 1.5	5.6 7.2	7.1 8.9	1.5 1.5	8.5 9.6	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

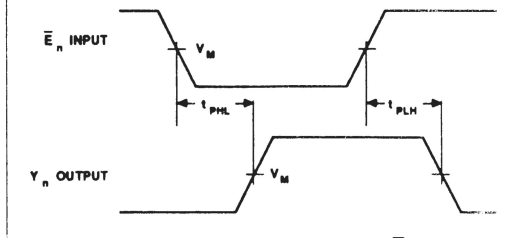
SYMBOL	PARAMETER	WAVEFORM	74ACT11238					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	5.1 6.1	7.1 7.8	1.5 1.5	7.8 8.6	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to Y_n	2	1.5 1.5	5.5 6.0	7.1 8.1	1.5 1.5	7.8 9.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y_n	2	1.5 1.5	5.4 7.1	7.6 8.8	1.5 1.5	8.3 9.7	ns

AC WAVEFORMS

AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V

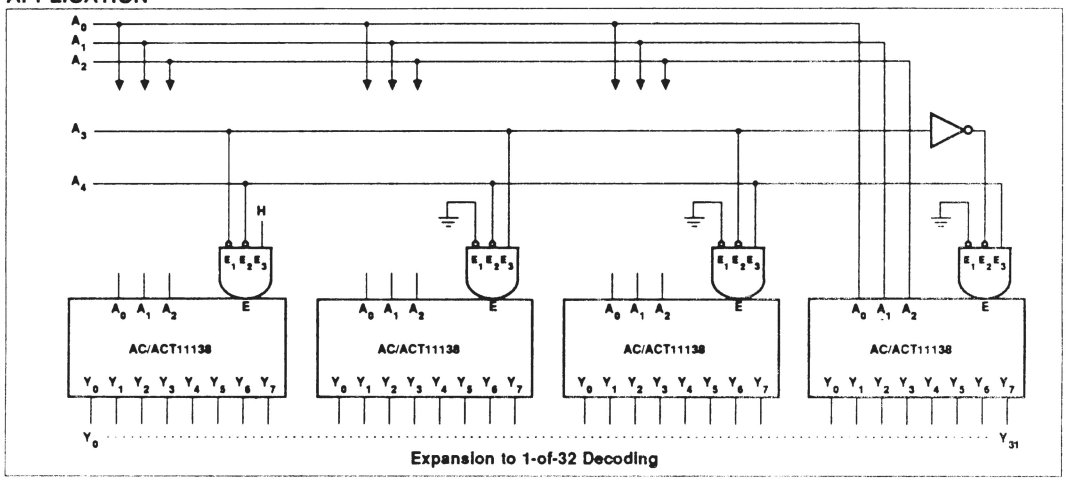


Waveform 1. Waveforms Showing the Inputs (A_n, E_3) to Output (Y_n) Propagation Delays



Waveform 2. Waveforms Showing the Input ($\overline{E}_n$) to Output (Y_n) Propagation Delays

APPLICATION



Expansion to 1-of-32 Decoding

74AC/ACT11240

Octal Buffer/Line Driver; 3-State; INV

Product Specification

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11240 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11240 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($\overline{OE}$), each controlling four of the 3-State outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF; V_{CC} = 5V	5.0	6.3	ns
C_{PD}	Power dissipation capacitance per buffer[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	39	47	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	12	13	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate; Data inputs	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

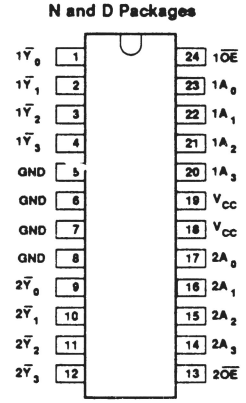
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

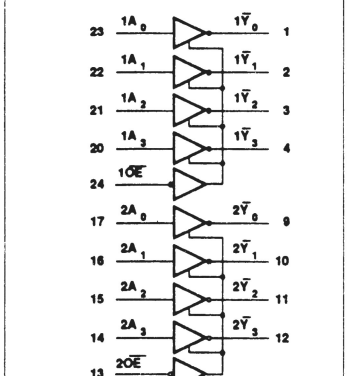
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11240N 74ACT11240N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11240D 74ACT11240D

PIN CONFIGURATION

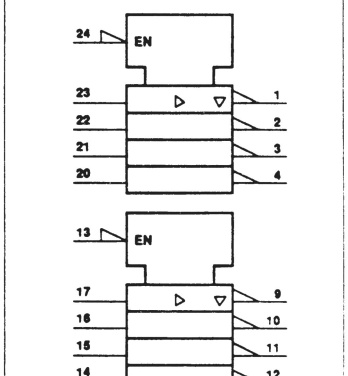
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
23, 22, 21, 20	$1I_0$ - $1I_3$	Data inputs
17, 16, 15, 14	$2I_0$ - $2I_3$	Data inputs
1, 2, 3, 4	$1\overline{Y}_0$ - $1\overline{Y}_3$	Data outputs
9, 10, 11, 12	$2\overline{Y}_0$ - $2\overline{Y}_3$	Data outputs
24, 13	$1\overline{OE}$, $2\overline{OE}$	Output enables
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	$2\overline{OE}$	$2A_n$	$1\overline{Y}_n$	$2\overline{Y}_n$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11240			74ACT11240			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]		3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11240				74ACT11240				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11240					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	7.6 6.3	10.5 8.6	1.5 1.5	11.7 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	8.2 7.6	11.6 10.8	1.5 1.5	12.7 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.5 6.7	7.5 9.4	1.5 1.5	7.8 9.8	ns

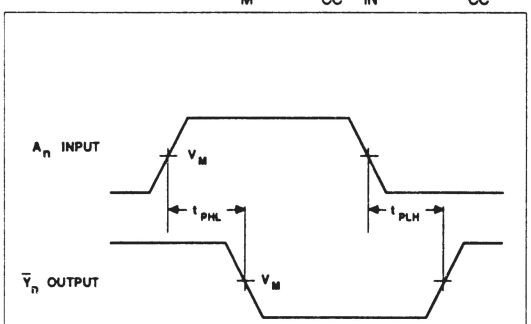
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11240					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	5.4 4.6	7.5 6.6	1.5 1.5	8.4 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.7 5.3	8.2 7.7	1.5 1.5	9.2 8.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.7 5.2	6.3 7.3	1.5 1.5	6.6 7.7	ns

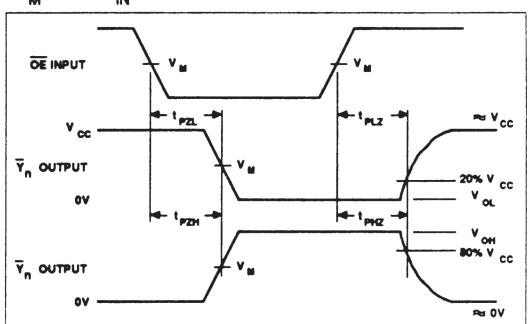
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11240					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	6.5 6.0	9.9 8.0	1.5 1.5	10.6 8.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	7.5 7.3	11.7 11.5	1.5 1.5	12.5 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	7.3 7.9	9.4 10.3	1.5 1.5	10.0 10.8	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (A_n) to Output ($\overline{Y}_n$) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11241

Octal Buffer/Line Driver; 3-State

Product Specification

FEATURES

- **Octal bus interface**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11241 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11241 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($1\overline{OE}$ and 2OE), each controlling four of the 3-State outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF; V_{CC} = 5V	4.7	6.5	ns
C_{PD}	Power dissipation capacitance per buffer[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	26	27	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	10	9	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate; Data inputs	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

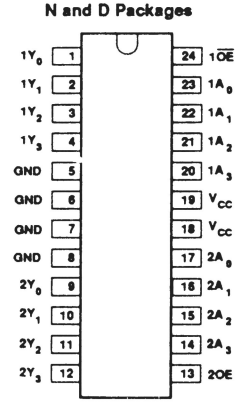
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times {V_{CC}}^2 \times f_I + \Sigma (C_L \times {V_{CC}}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times {V_{CC}}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

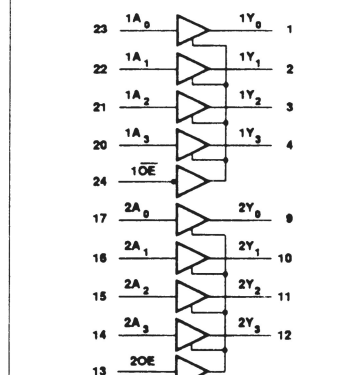
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11241N 74ACT11241N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11241D 74ACT11241D

PIN CONFIGURATION

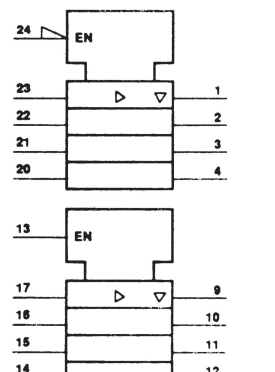
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
23, 22, 21, 20	$1A_0$ - $1A_3$	Data inputs
17, 16, 15, 14	$2A_0$ - $2A_3$	Data inputs
1, 2, 3, 4	$1Y_0$ - $1Y_3$	Data outputs
9, 10, 11, 12	$2Y_0$ - $2Y_3$	Data outputs
24, 13	$1\overline{OE}$, 2OE	Output enables
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	2OE	$2A_n$	$1Y_n$	$2Y_n$
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11241			74ACT11241			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]		3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11241				74ACT11241				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11241					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	7.0 6.2	10.0 8.4	1.5 1.5	11.4 9.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.8 7.7	11.4 10.6	1.5 1.5	12.9 11.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	5.8 7.1	7.6 9.3	1.5 1.5	7.9 9.9	ns

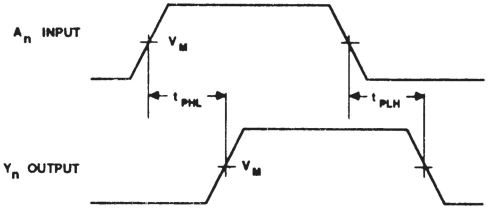
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11241					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	4.9 4.5	7.1 6.3	1.5 1.5	8.0 6.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.4 5.3	8.0 7.6	1.5 1.5	9.0 8.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	4.9 5.6	6.6 7.5	1.5 1.5	6.9 8.0	ns

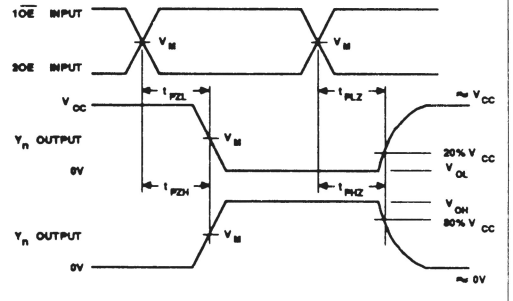
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11241					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	6.6 6.3	9.0 8.5	1.5 1.5	10.0 9.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.4	11.3 10.5	1.5 1.5	12.3 11.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.6 8.2	10.6 11.2	1.5 1.5	11.0 11.7	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (A_n) to Output (Y_n) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11244

Octal Buffer/Line Driver; 3-State

Product Specification

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11244 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11244 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF; V_{CC} = 5V	4.7	5.7	ns
C_{PD}	Power dissipation capacitance per buffer[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	27	27	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	9	9	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate; Data inputs	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

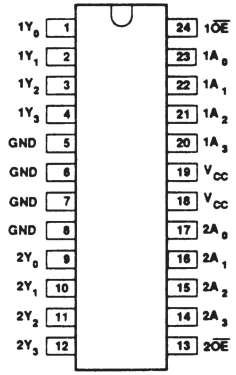
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

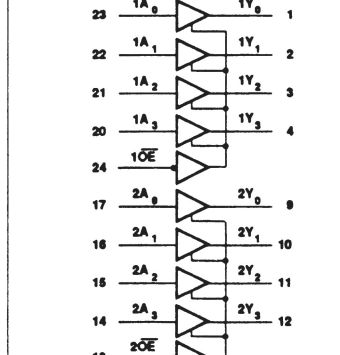
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11244N 74ACT11244N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11244D 74ACT11244D

PIN CONFIGURATION

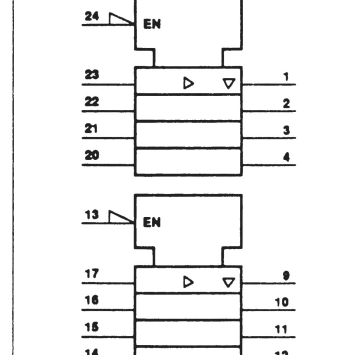
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
23, 22, 21, 20	$1A_0$ - $1A_3$	Data inputs
17, 16, 15, 14	$2A_0$ - $2A_3$	Data inputs
1, 2, 3, 4	$1Y_0$ - $1Y_3$	Data outputs
9, 10, 11, 12	$2Y_0$ - $2Y_3$	Data outputs
24, 13	$1\overline{OE}$, $2\overline{OE}$	Output enables
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1I_n$	$2\overline{OE}_b$	$2I_n$	$1Y_n$	$2Y_n$
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11244			74ACT11244			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]		3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11244				74ACT11244				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11244					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	7.1 6.3	9.3 8.6	1.5 1.5	10.2 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.0 7.9	10.7 10.6	1.5 1.5	11.8 11.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	5.9 7.2	7.9 9.4	1.5 1.5	8.3 9.9	ns

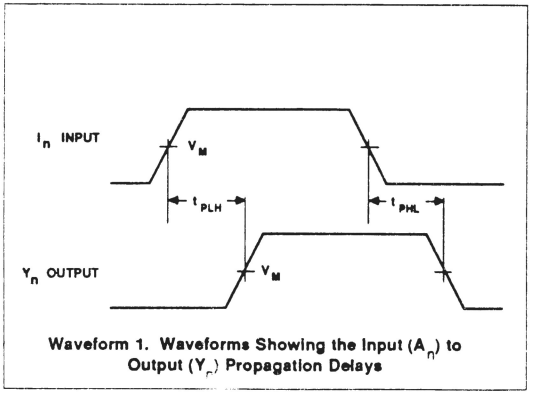
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11244					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	4.9 4.5	6.7 6.4	1.5 1.5	7.3 6.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.4 5.4	7.7 7.6	1.5 1.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	5.2 5.8	7.0 7.8	1.5 1.5	7.3 8.2	ns

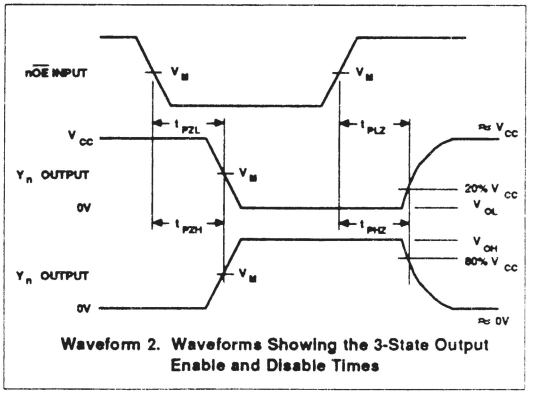
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $_R = t_{F\,f}$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11244					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.5 1.5	6.0 5.4	8.9 8.6	1.5 1.5	9.9 9.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.6 6.7	11.3 10.5	1.5 1.5	12.5 11.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.4 7.8	9.8 10.6	1.5 1.5	10.4 11.2	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (A_n) to Output (Y_n) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11245

Octal Transceiver with Direction Pin; 3-State

Product Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11245 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11245 device is an octal transceiver featuring noninverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V	4.5	5.8	ns
C_{PD}	Power dissipation capacitance per buffer[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	64	66	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	16	19	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
C_{IO}	I/O capacitance	V_I = 0V or V_{CC}	12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:

   f_I = input frequency in MHz, C_L = output load capacitance in pF,

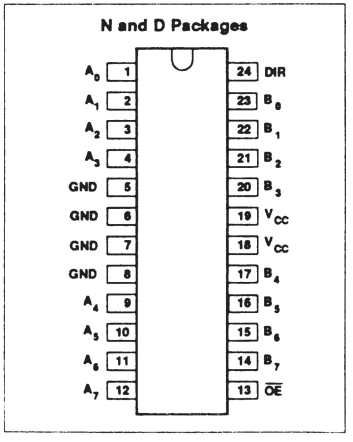
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,

   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

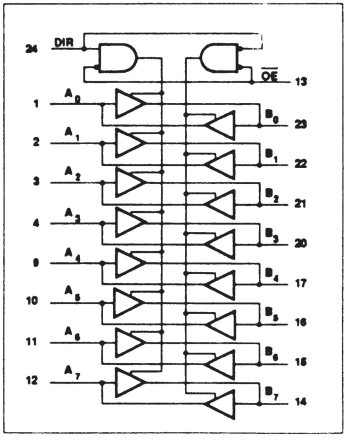
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11245N 74ACT11245N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11245D 74ACT11245D

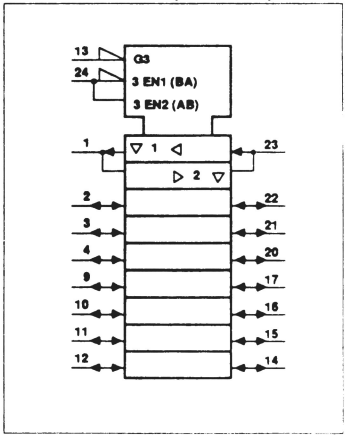
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	DIR	Direction control input
1, 2, 3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
13	$\overline{OE}$	Output enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11245			74ACT11245			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11245				74ACT11245				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11245					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	6.5 5.7	11.2 8.5	1.5 1.5	12.5 9.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.6 8.2	14.2 11.5	1.5 1.5	15.9 12.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.7 8.5	10.5 12.0	1.5 1.5	11.3 13.0	ns

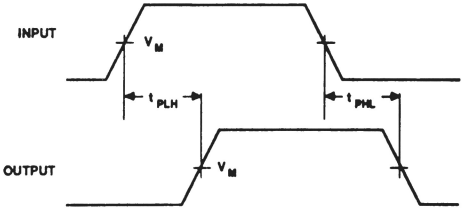
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11245					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	4.8 4.1	8.5 6.3	1.5 1.5	9.5 6.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.2 5.9	10.2 8.6	1.5 1.5	11.4 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	6.4 7.0	8.8 9.6	1.5 1.5	9.5 10.4	ns

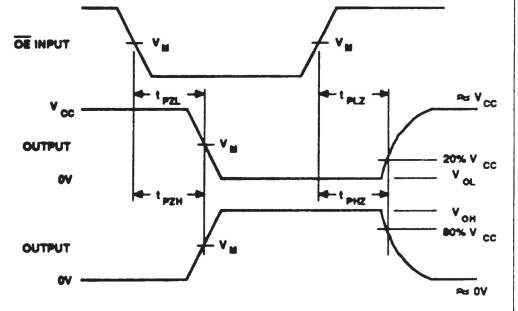
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11245					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	6.2 5.4	9.2 8.6	1.5 1.5	10.0 9.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.1 8.2	12.0 11.7	1.5 1.5	13.2 12.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.3 9.8	11.8 12.9	1.5 1.5	12.9 13.9	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input to Output Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11251
8-Input Multiplexer (3-State)

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11251 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11251 provides an 8-to-1 multiplexer with three select lines and a common output enable. The state of the Select (S_n) inputs determines the particular input line from which the data comes. The Output Enable ($\overline{OE}$) input is active-Low. When $\overline{OE}$ is High, both the Y output and the $\overline{Y}$ output are in the High-impedance "OFF" state regardless of all other input conditions.

The device is the logic implementation of a single pole, 8 position switch where the position of the switch is determined by the logic levels supplied to the Select inputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay I_n to Y	C_L = 50pF; V_{CC} = 5V	4.8	6.6	ns
C_{PD}	Power dissipation capacitance[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	55	60	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	13	16	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled	8.0	8.0	pF
$\Delta t/\Delta v$	Maximum input rise or fall rate; Data inputs	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

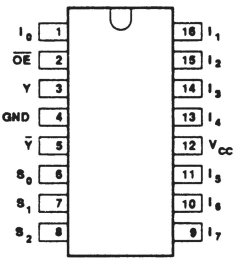
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

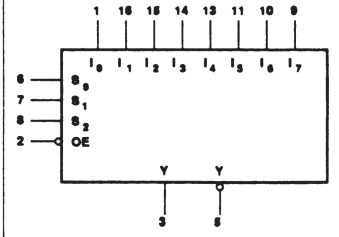
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11251N 74ACT11251N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11251D 74ACT11251D

PIN CONFIGURATION

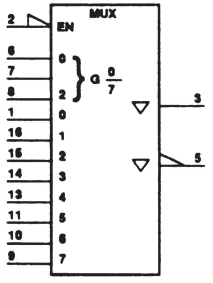
N and D Packages



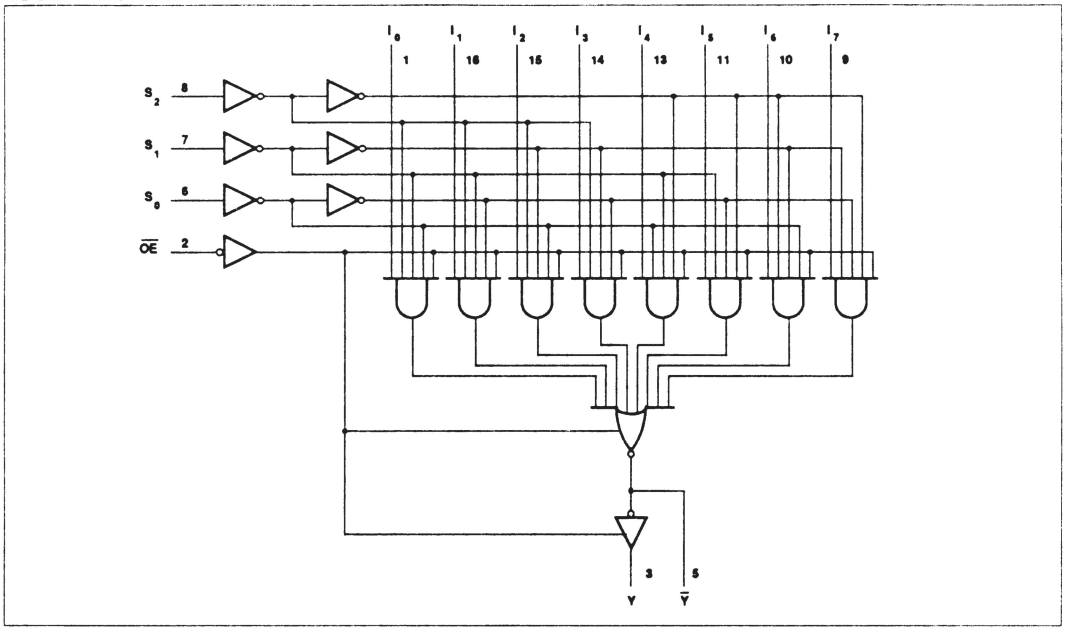
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
6, 7, 8	S_n	Select inputs
2	$\overline{OE}$	Output enable input
1, 16, 15, 14 13, 11, 10, 9	$I_0 - I_7$	Data inputs
3, 5	Y, $\overline{Y}$	Data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11151			74ACT11151			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11251				74ACT11251				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11251					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	1.5 1.5	7.0 6.9	8.6 8.3	1.5 1.5	9.3 8.9	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.5 1.5	6.1 6.6	7.5 8.0	1.5 1.5	8.1 8.8	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	1	1.5 1.5	10.0 9.6	11.6 11.1	1.5 1.5	12.6 12.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	1	1.5 1.5	8.9 9.6	10.4 11.1	1.5 1.5	11.3 12.1	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	4.6 5.5	5.9 6.8	1.5 1.5	6.3 7.2	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	4.1 5.0	5.4 6.3	1.5 1.5	5.8 6.8	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	4.3 5.0	5.5 6.2	1.5 1.5	5.7 6.4	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	4.0 4.4	5.1 5.6	1.5 1.5	5.4 5.8	ns

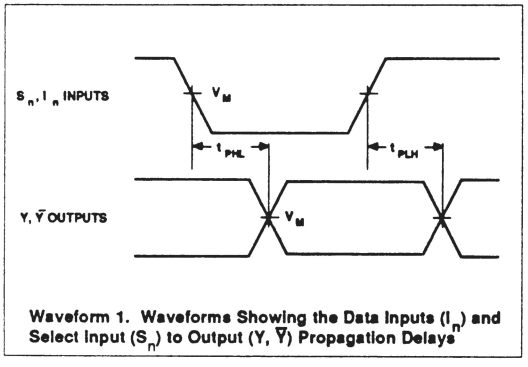
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11251					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	1.5 1.5	4.8 4.7	6.1 6.0	1.5 1.5	6.7 6.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.5 1.5	4.1 4.5	5.4 5.9	1.5 1.5	5.8 6.4	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	1	1.5 1.5	6.6 6.5	7.9 7.8	1.5 1.5	8.6 8.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	1	1.5 1.5	5.9 6.3	7.2 7.7	1.5 1.5	7.8 8.4	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	3.2 3.8	4.5 5.1	1.5 1.5	4.7 5.4	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	2.9 3.5	4.2 4.8	1.5 1.5	4.4 5.1	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	4.0 4.4	5.3 5.6	1.5 1.5	5.4 5.9	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	3.6 3.7	4.8 4.9	1.5 1.5	5.0 5.1	ns

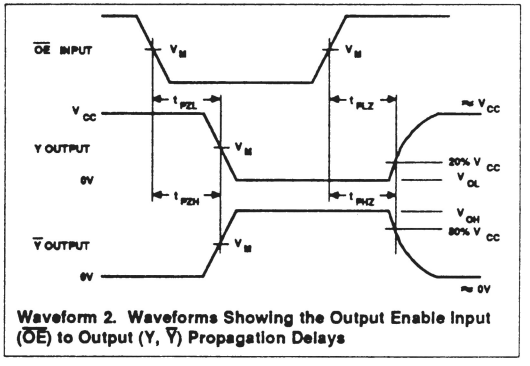
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11251					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	1.5 1.5	6.4 6.7	7.8 8.1	1.5 1.5	8.5 8.7	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.5 1.5	6.0 5.9	7.4 7.3	1.5 1.5	7.9 7.9	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	1	1.5 1.5	9.3 8.2	10.9 9.8	1.5 1.5	11.8 10.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	1	1.5 1.5	7.8 8.8	9.5 10.4	1.5 1.5	10.2 11.4	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	5.3 4.8	6.7 6.2	1.5 1.5	7.0 6.6	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	5.2 4.7	6.5 6.0	1.5 1.5	7.0 6.4	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	2	1.5 1.5	6.0 5.2	7.3 6.4	1.5 1.5	7.7 6.7	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.5 1.5	5.9 4.9	7.2 6.2	1.5 1.5	7.6 6.4	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Data Inputs (I_n) and Select Input (S_n) to Output (Y, $\overline{Y}$) Propagation Delays



Waveform 2. Waveforms Showing the Output Enable Input ($\overline{OE}$) to Output (Y, $\overline{Y}$) Propagation Delays

74AC/ACT11253

Dual 4-Input Multiplexer; 3-State

Product Specification

FEATURES

- **3-State outputs for bus interface and multiplex expansion**
- **Separate 3-State Output Enable inputs**
- **Common Select inputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11253 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11253 device provides two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common select inputs (S_0, S_1). When the individual output enable ($1\overline{OE}$, $2\overline{OE}$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance state.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay $1I_n$, $2I_n$ to nY	C_L = 50pF; V_{CC} = 5V	4.7	6.5	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	35	41	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	11	15	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled	8	8	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

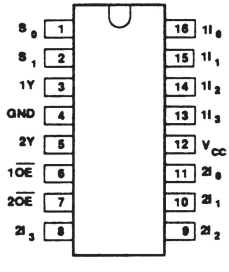
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

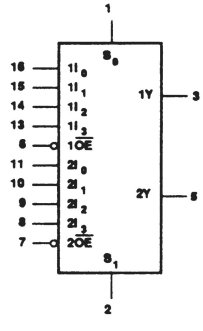
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11253N 74ACT11253N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11253D 74ACT11253D

PIN CONFIGURATION

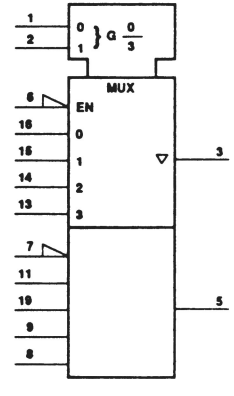
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The 74AC/ACT11253 devices are the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two select inputs.

The '11253 is the non-inverting version of the '11353.

PIN DESCRIPTION

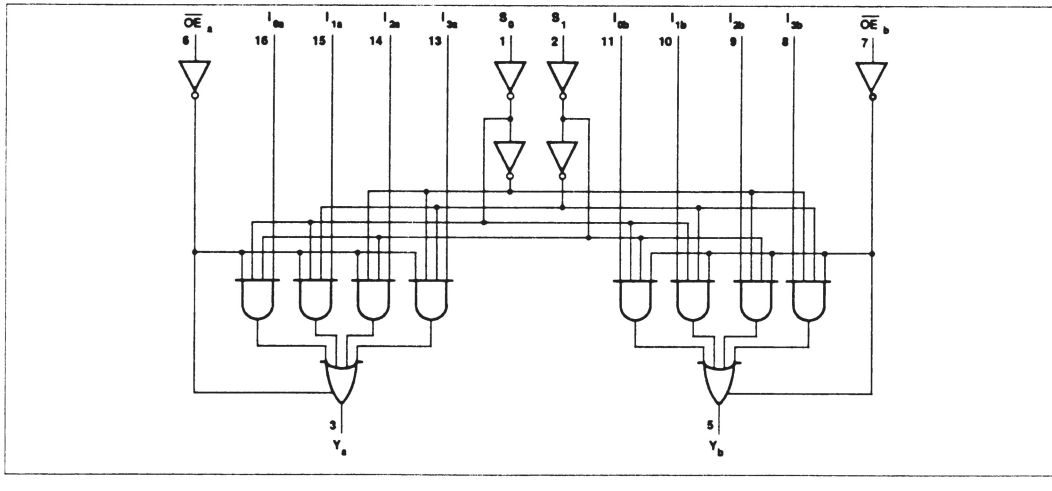
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2	S_0, S_1	Common select inputs
16, 15, 14, 13	$1I_0$ - $1I_3$	Port A data inputs
11, 10, 9, 8	$2I_0$ - $2I_3$	Port B data inputs
6	$1\overline{OE}$	Port A output enable input
7	$2\overline{OE}$	Port B output enable input
3, 5	1Y, 2Y	3-State data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUT
$\overline{OE}_n$	S_0	S_1	I_{0n}	I_{1n}	I_{2n}	I_{3n}	Y_n
H	X	X	X	X	X	X	Z
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
L	H	L	X	L	X	X	L
L	H	L	X	H	X	X	H
L	L	H	X	X	L	X	L
L	L	H	X	X	H	X	H
L	H	H	X	X	X	L	L
L	H	H	X	X	X	H	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
Z = High-impedance "OFF" state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11253			74ACT11253			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11253				74ACT11253				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11253					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to nY	1	1.5 1.5	6.8 7.0	8.3 8.8	1.5 1.5	9.3 9.6	ns
t_{PLH} t_{PHL}	Propagation delay nS to nY	1	1.5 1.5	7.1 7.5	9.7 10.1	1.5 1.5	11.0 11.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	4.8 5.8	6.2 7.4	1.5 1.5	6.8 8.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	5.0 5.2	6.3 6.5	1.5 1.5	6.7 6.9	ns

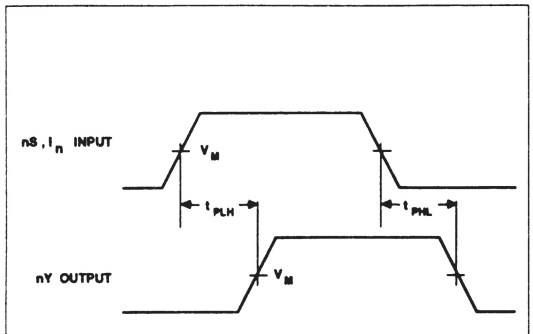
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11253					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to nY	1	1.5 1.5	4.5 4.8	5.9 6.3	1.5 1.5	6.6 6.9	ns
t_{PLH} t_{PHL}	Propagation delay nS to nY	1	1.5 1.5	4.9 5.2	7.0 7.3	1.5 1.5	7.9 8.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	3.4 4.0	4.6 5.3	1.5 1.5	5.1 5.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	4.7 4.6	6.0 5.9	1.5 1.5	6.3 6.2	ns

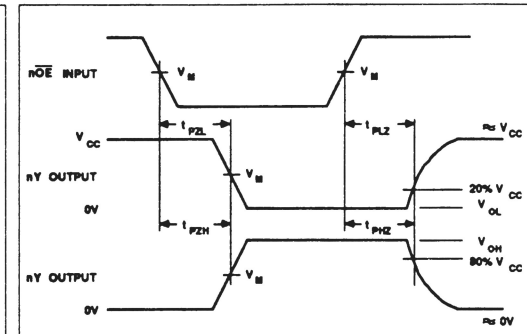
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11253					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to nY	1	1.5 1.5	5.7 7.2	7.4 10.5	1.5 1.5	8.3 11.7	ns
t_{PLH} t_{PHL}	Propagation delay nS to nY	1	1.5 1.5	6.8 9.1	9.8 12.6	1.5 1.5	11.0 14.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.0 4.8	7.6 7.3	1.5 1.5	8.5 8.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	6.4 5.9	8.6 7.4	1.5 1.5	9.2 7.8	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (I_n and nS) to Output (nY) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11257
Quad 2-Input Multiplexer (3-State)

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11257 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11257 provides four 2-to-1 multiplexers with 3-State outputs which have a common selector and a common output enable. The state of the Select (S) input determines the particular register from which the data comes. The Output Enable ($\overline{OE}$) input is active-Low. When $\overline{E}$ is High, all of the outputs (Y) are forced to a High-impedance state regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
		T_A = 25°C; GND = 0V	AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay nI_0, nI_1 to nY	C_L = 50pF; V_{CC} = 5V	4.3	5.7	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	37	41	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	11	14	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled	8.0	8.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

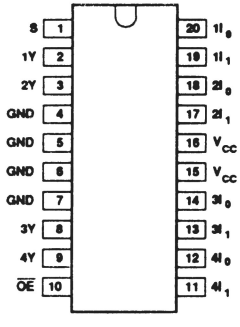
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

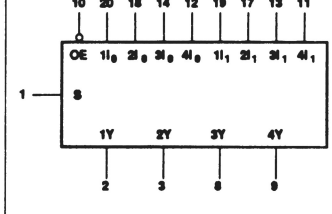
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11257N 74ACT11257N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11257D 74ACT11257D

PIN CONFIGURATION

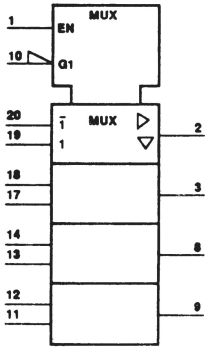
N and D Packages



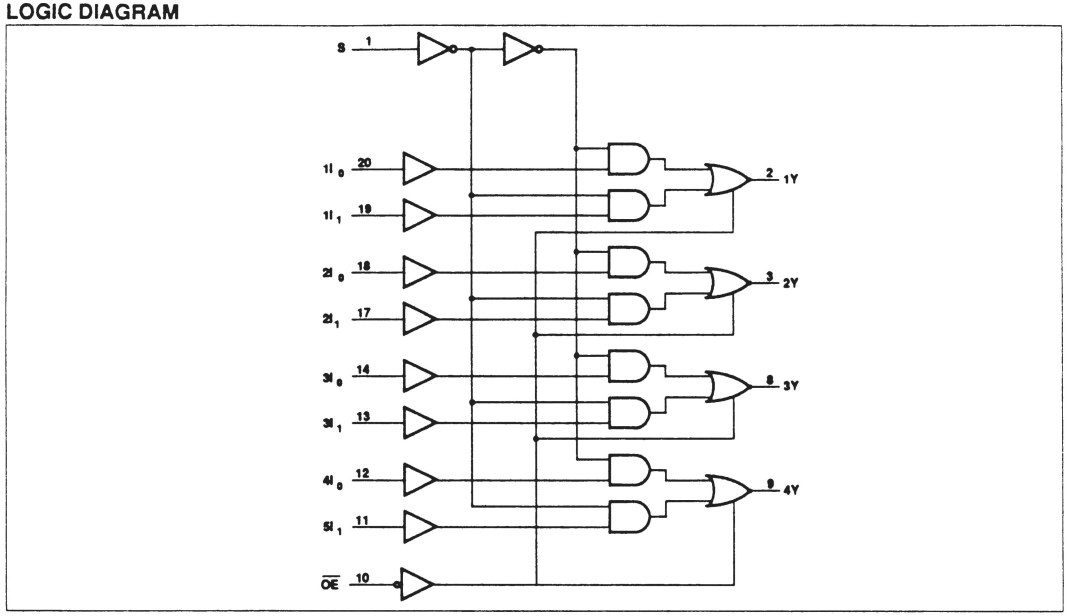
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	nI_0 - nI_0	Data inputs
19, 17, 13, 11	nI_1 - nI_1	Data inputs
2, 3, 8, 9	1Y - 4Y	Data outputs
10	$\overline{OE}$	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{OE}$	S	nI_0	nI_1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11257			74ACT1257			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11257				74ACT11257				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11257					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to nY	1	1.5 1.5	5.8 6.6	8.0 9.1	1.5 1.5	8.8 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S to nY	1	1.5 1.5	6.7 7.5	9.2 10.1	1.5 1.5	10.0 11.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.9 7.5	8.2 10.7	1.5 1.5	8.8 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	6.1 6.8	8.0 8.9	1.5 1.5	8.5 9.6	ns

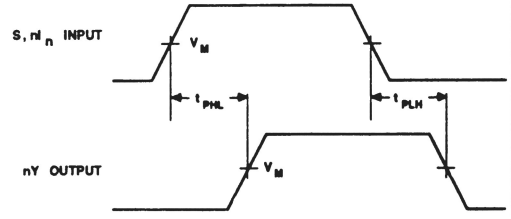
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11257					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to nY	1	1.5 1.5	3.9 4.6	5.7 6.5	1.5 1.5	6.1 7.1	ns
t_{PLH} t_{PHL}	Propagation delay S to nY	1	1.5 1.5	4.5 5.2	6.4 7.4	1.5 1.5	7.0 8.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	4.1 5.2	5.8 7.5	1.5 1.5	6.2 8.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.1 5.5	6.7 7.1	1.5 1.5	7.1 7.6	ns

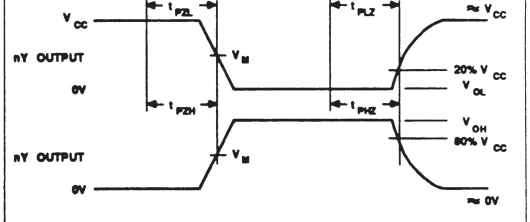
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11257					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to nY	1	1.5 1.5	5.2 6.2	7.0 8.9	1.5 1.5	7.5 9.7	ns
t_{PLH} t_{PHL}	Propagation delay S to nY	1	1.5 1.5	6.1 6.9	8.5 9.0	1.5 1.5	9.2 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.2 6.4	7.5 9.1	1.5 1.5	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	6.5 6.8	8.2 8.4	1.5 1.5	8.9 9.2	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nI_n, S) to Output (nY) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11258

Quad 2-Input Multiplexer (3-State), Inverting

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11258 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11258 provides four 2-to-1 multiplexers with 3-State inverting outputs which have a common selector and a common output enable. The state of the Select (S) input determines the particular register from which the data comes. The Output Enable ($\overline{OE}$) input is active-Low. When $\overline{E}$ is High, all of the outputs ($\overline{Y}$) are forced to a High-impedance state regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	C_L = 50pF; V_{CC} = 5V	4.1	5.4	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	33	35	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	13	16	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled	9	9	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

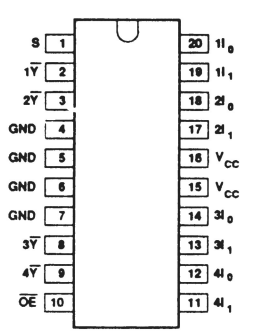
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

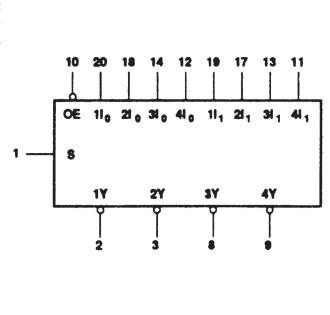
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11258N 74ACT11258N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11258D 74ACT11258D

PIN CONFIGURATION

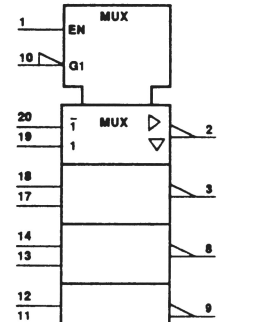
N and D Packages



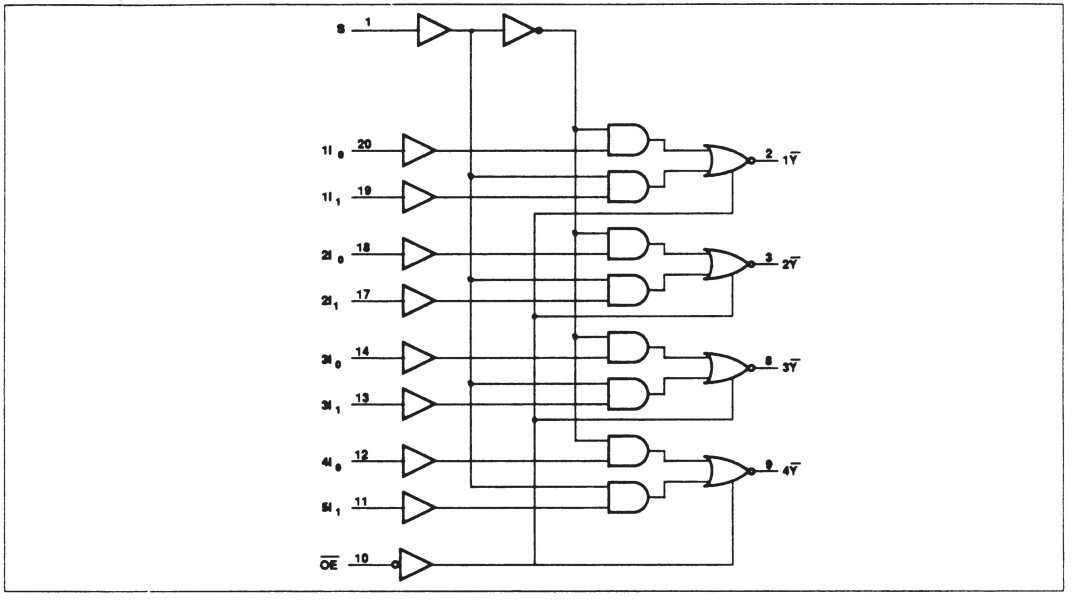
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	nI_0 - nI_0	Data inputs
19, 17, 13, 11	nI_1 - nI_1	Data inputs
2, 3, 8, 9	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
10	$\overline{OE}$	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{OE}$	S	nI_0	nI_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11258			74ACT1258			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11258				74ACT11258				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11258					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	5.4 6.2	6.8 7.7	1.5 1.5	7.3 8.4	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	6.1 6.9	7.6 8.5	1.5 1.5	8.1 9.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.3 6.9	6.7 8.6	1.5 1.5	7.2 9.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.6 6.1	7.0 7.8	1.5 1.5	7.4 8.5	ns

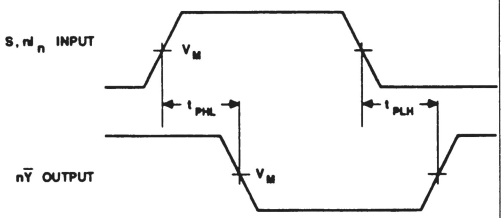
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11258					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	3.7 4.4	5.0 6.0	1.5 1.5	5.3 6.7	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	4.2 4.9	5.5 6.5	1.5 1.5	5.8 7.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	3.7 4.8	5.0 6.4	1.5 1.5	5.2 7.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.6 4.9	6.0 6.5	1.5 1.5	6.3 7.1	ns

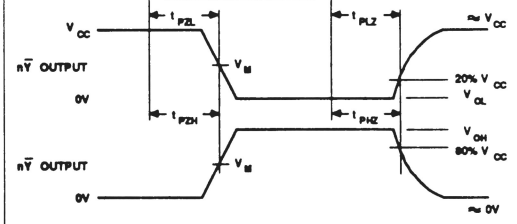
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11258					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	5.4 5.3	7.0 7.0	1.5 1.5	7.4 7.8	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	5.7 6.6	7.2 8.3	1.5 1.5	7.7 9.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.0 6.0	6.4 7.7	1.5 1.5	6.8 8.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.9 6.2	7.3 7.8	1.5 1.5	7.7 8.5	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nI_n, S) to Output ($n\overline{Y}$) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11280

9-Bit Odd/Even Parity Generator/Checker

Preliminary Specification

FEATURES

- **Word length easily expanded by cascading**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11280 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11280 9-bit parity generator or checker is commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is High when an even number of Data inputs (I_0 - I_8) is High. The Odd parity output (Σ_O) is High when an odd number of Data inputs are High.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay I_n to Σ_n	C_L = 50pF; V_{CC} = 5V	6.9	7.7	ns
C_{PD}	Power dissipation capacitance[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	55	65	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

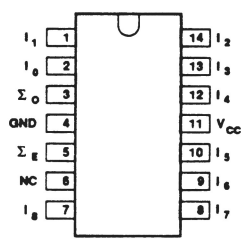
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11280N 74ACT11280N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11280D 74ACT11280D

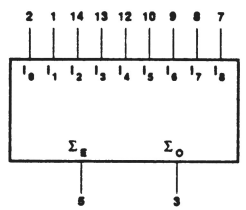
Expansion to larger word sizes is accomplished by tying the Even outputs of up to nine parallel devices to the data inputs of the final stage.

PIN CONFIGURATION

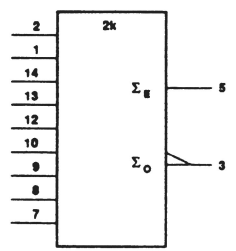
N and D Packages



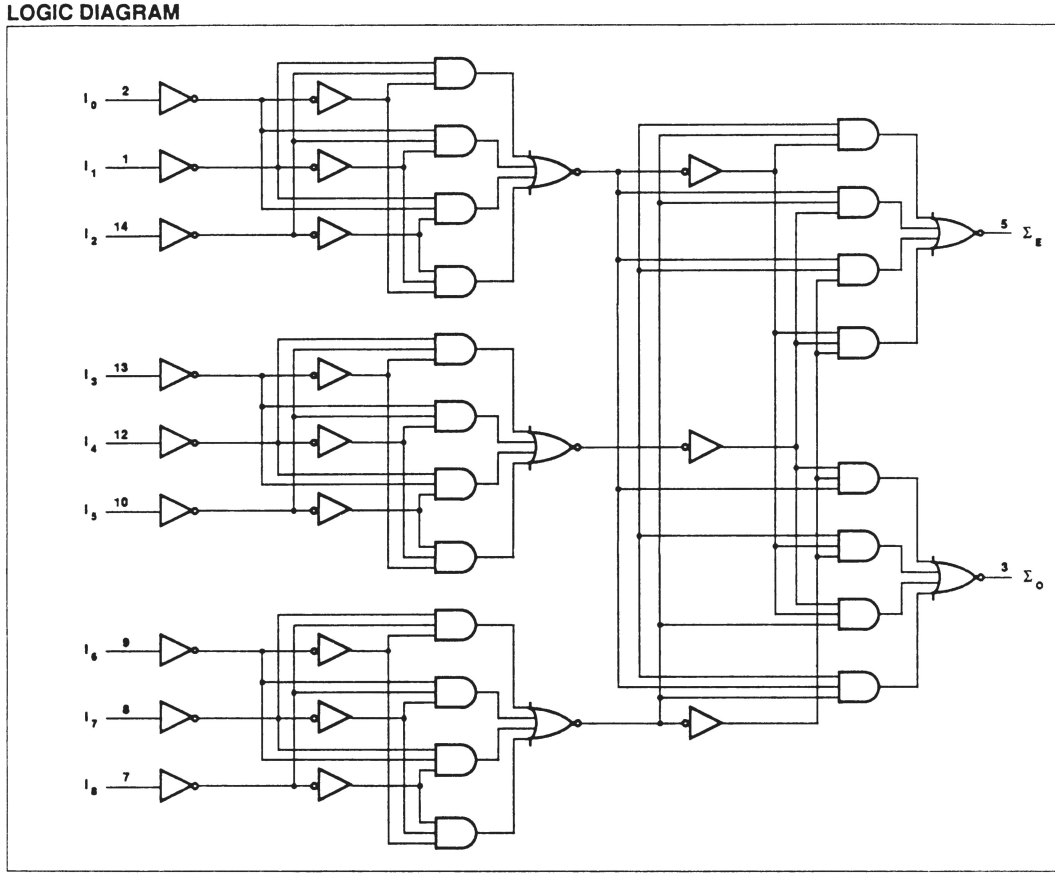
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 1, 14, 13, 12, 10, 9, 8, 7	I_0 - I_8	Data inputs
5	Σ_E	Even parity output
3	Σ_O	Odd parity output
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS	OUTPUTS	
Number of High Data Inputs (I_0 - I_8)	Σ_E	Σ_O
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H

H = High voltage level
L = Low voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11280			74ACT11280			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11280				74ACT11280				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11280					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E	1	1.5 1.5	10.2 11.5	11.8 13.0	1.5 1.5	12.9 14.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_O	1	1.5 1.5	11.0 11.4	12.5 12.8	1.5 1.5	13.7 14.0	ns

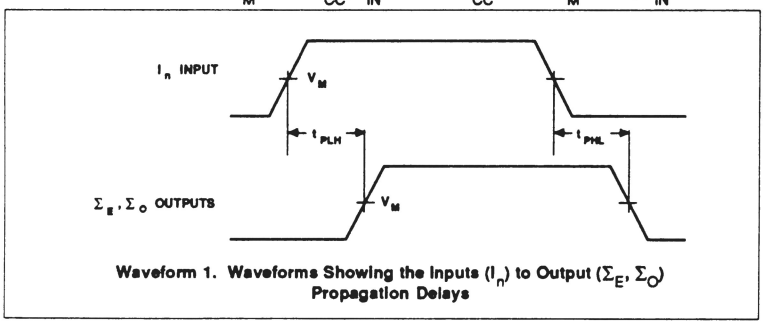
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11280					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E	1	1.5 1.5	6.1 7.2	8.3 9.5	1.5 1.5	9.1 10.4	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_O	1	1.5 1.5	6.6 7.5	8.9 9.7	1.5 1.5	9.7 10.6	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11280					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E	1	1.5 1.5	7.5 8.0	11.2 10.6	1.5 1.5	12.3 11.8	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_O	1	1.5 1.5	7.4 8.0	10.8 10.4	1.5 1.5	11.9 11.6	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Inputs (I_n) to Output (Σ_E, Σ_O) Propagation Delays

74AC/ACT11286

9-Bit Odd/Even Parity Generator/Checker with Bus Drive I/O Port

Preliminary Specification

FEATURES

- **Generates either odd or even parity for nine data lines**
- **Word length easily expanded by cascading**
- **Direct bus connection for parity generation or for checking by using the parity I/O port**
- **Glitch-free bus during power up/down**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11286 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11286 9-bit parity generator or checker is commonly used to detect errors in high-speed data transmission or data retrieval systems. It features a local output for parity checking and a bus-driv-

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay I_n to PARITY ERROR	C_L = 50pF; V_{CC} = 5V	6.9	8.6	ns
C_{PD}	Power dissipation capacitance[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	53	56	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	46	50	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled	8.5	8.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

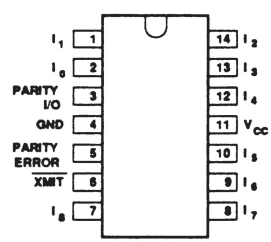
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

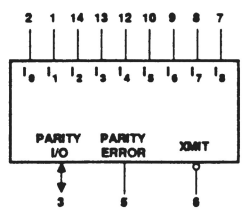
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11286N 74ACT11286N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11286D 74ACT11286D

PIN CONFIGURATION

N and D Packages



LOGIC SYMBOL



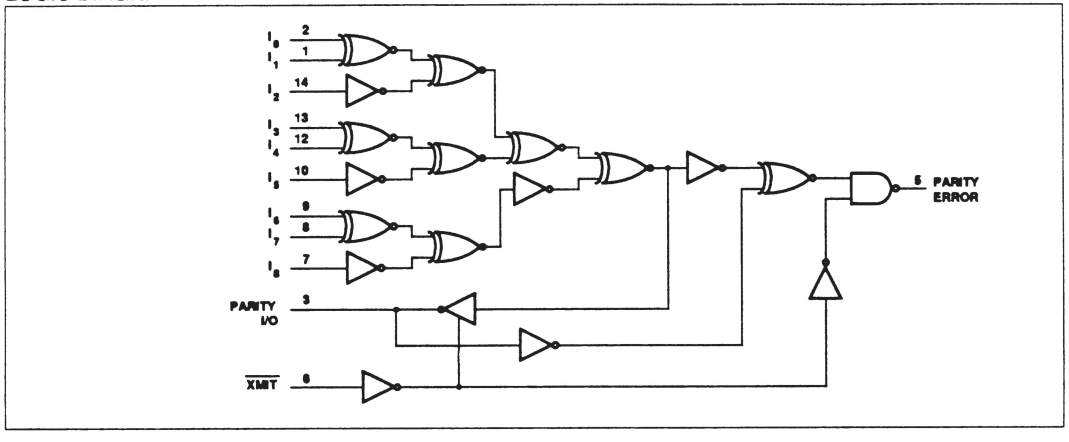
LOGIC SYMBOL (IEEE/IEC)

ing parity I/O port for parity generation/checking.

The $\overline{XMIT}$ control input is implemented specifically for cascading for expanding word length. When $\overline{XMIT}$ is held Low the parity tree is disabled and the Parity Error output remains at a High logic level regardless of the other inputs (I_0 - I_8). When $\overline{XMIT}$ is High the parity tree is enabled. Parity Error indicates a parity error when either an even number of inputs are High and Parity I/O is forced to Low, or when an odd number of inputs are High and Parity I/O is forced High.

The I/O control circuitry is designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 1, 14, 13, 12, 10, 9, 8, 7	I_0 - I_8	Data inputs
3	PARITY I/O	Parity I/O
6	$\overline{XMIT}$	Transmit input (active Low)
5	PARITY ERROR	Parity error output
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

Number of High Data Inputs (I_0 - I_8)	$\overline{XMIT}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	H
1, 3, 5, 7, 9	h	h	L
	h	l	H

l = Low voltage level input
h = High voltage level input
H = High voltage level output
L = Low voltage level output

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11286			74ACT11286			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11286				74ACT11286				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11286					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY I/O	1	1.5 1.5	9.3 10.6	13.2 14.5	1.5 1.5	15.2 17.2	ns
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY ERROR	1	1.5 1.5	10.1 11.0	14.4 15.1	1.5 1.5	16.3 17.1	ns
t_{PLH} t_{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	1.5 1.5	6.4 7.3	8.7 9.5	1.5 1.5	9.6 10.7	ns
t_{PZH} t_{PHZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	5.0 4.8	6.8 6.2	1.5 1.5	7.5 6.5	ns
t_{PZL} t_{PLZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	9.1 5.4	11.9 6.9	1.5 1.5	13.1 7.4	ns

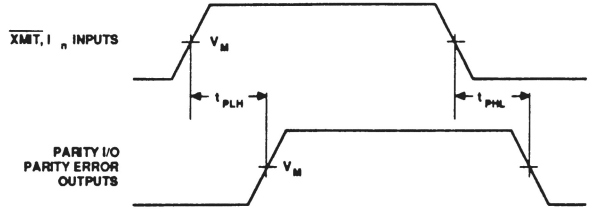
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11286					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY I/O	1	1.5 1.5	6.0 6.9	8.8 9.8	1.5 1.5	10.0 11.1	ns
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY ERROR	1	1.5 1.5	6.6 7.2	9.4 10.1	1.5 1.5	10.6 11.4	ns
t_{PLH} t_{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	1.5 1.5	4.4 5.0	6.1 6.7	1.5 1.5	6.8 7.4	ns
t_{PZH} t_{PHZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	3.4 4.4	5.0 5.7	1.5 1.5	5.4 6.0	ns
t_{PZL} t_{PLZ}	Propagation delay. $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	5.7 4.6	7.9 5.9	1.5 1.5	9.0 6.3	ns

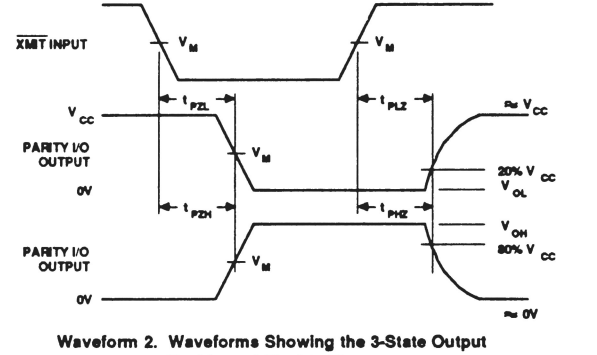
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11286					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY I/O	1	1.5 1.5	7.8 8.8	10.6 11.6	1.5 1.5	12.1 13.3	ns
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY ERROR	1	1.5 1.5	8.3 8.8	11.1 11.9	1.5 1.5	12.7 13.4	ns
t_{PLH} t_{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	1.5 1.5	6.0 6.7	7.8 8.3	1.5 1.5	8.5 9.2	ns
t_{PZH} t_{PHZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	5.3 6.7	7.4 7.9	1.5 1.5	8.0 8.5	ns
t_{PZL} t_{PLZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.5 1.5	7.9 6.8	10.5 8.0	1.5 1.5	11.6 8.7	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Inputs (I_n, $\overline{XMIT}$) to Outputs (PARITY ERROR, PARITY I/O) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11353

Dual 4-Input Multiplexer; 3-State; INV

Product Specification

FEATURES

- **3-State outputs for bus interface and multiplex expansion**
- **Separate 3-State Output Enable inputs**
- **Common Select inputs**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11353 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11353 device provides two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common select inputs (S_0, S_1). When the individual output enable ($1\overline{OE}$, $2\overline{OE}$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance state.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
		T_A = 25°C; GND = 0V	AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay $1I_n$, $2I_n$ to $n\overline{Y}$	C_L = 50pF; V_{CC} = 5V	4.6	5.8	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	31	39	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	12	19	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled	8	8	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = C_{PD} \times {V_{CC}}^2 \times f_I + \Sigma\,(C_L \times {V_{CC}}^2 \times f_O)$$ where:

f_I = input frequency in MHz, C_L = output load capacitance in pF,

f_O = output frequency in MHz, V_{CC} = supply voltage in V,

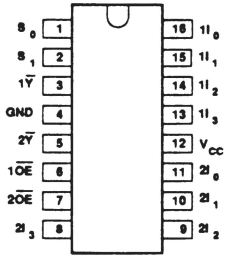
$\Sigma\,(C_L \times {V_{CC}}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

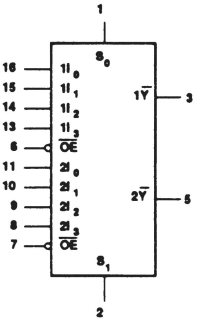
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11353N 74ACT11353N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11353D 74ACT11353D

PIN CONFIGURATION

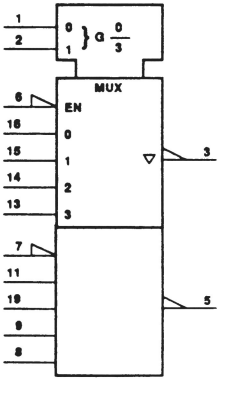
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The 74AC/ACT11353 devices are the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two select inputs.

The '11253 is the non-inverting version of the '11353.

PIN DESCRIPTION

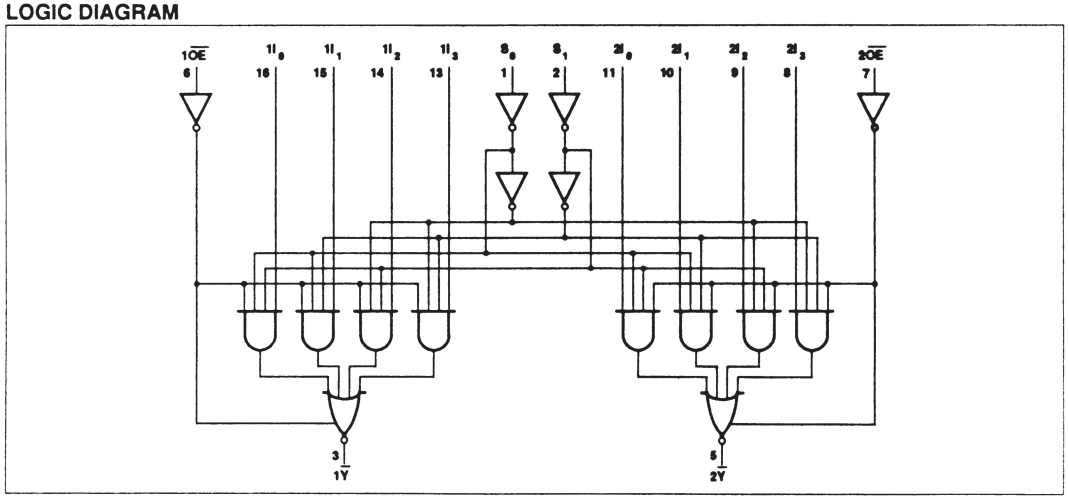
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2	S_0, S_1	Common select inputs
16, 15, 14, 13	$1I_0$ - $1I_3$	Port A data inputs
11, 10, 9, 8	$2I_0$ - $2I_3$	Port B data inputs
6	$1\overline{OE}$	Port A output enable input
7	$2\overline{OE}$	Port B output enable input
3, 5	$1\overline{Y}$, $2\overline{Y}$	3-State data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUT
$n\overline{OE}$	S_0	S_1	nI_0	nI_1	nI_2	nI_3	$n\overline{Y}$
H	X	X	X	X	X	X	Z
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
L	H	L	X	L	X	X	H
L	H	L	X	H	X	X	L
L	L	H	X	X	L	X	H
L	L	H	X	X	H	X	L
L	H	H	X	X	X	L	H
L	H	H	X	X	X	H	L

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
Z = High-impedance "OFF" state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11353			74ACT11353			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11353				74ACT11353				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11353					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_n to $n\overline{Y}$	1	1.5 1.5	6.5 6.6	8.6 8.7	1.5 1.5	9.6 9.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $n\overline{Y}$	1	1.5 1.5	7.0 7.2	9.6 9.8	1.5 1.5	10.7 10.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	4.4 5.4	6.0 7.2	1.5 1.5	6.6 7.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.8 4.9	6.2 6.3	1.5 1.5	6.5 6.6	ns

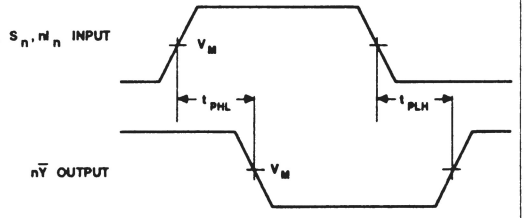
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11353					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_n to $n\overline{Y}$	1	1.5 1.5	4.5 4.6	5.9 6.1	1.5 1.5	6.6 6.8	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $n\overline{Y}$	1	1.5 1.5	4.0 4.2	6.6 6.9	1.5 1.5	7.4 7.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	2.9 3.4	4.4 5.1	1.5 1.5	4.8 5.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.4 4.1	5.8 5.5	1.5 1.5	6.1 5.8	ns

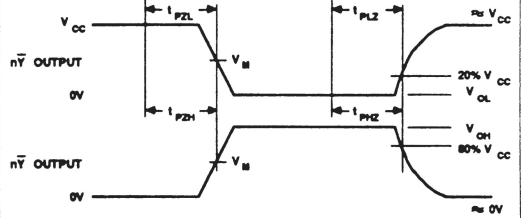
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11353					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_n to $n\overline{Y}$	1	1.5 1.5	6.3 5.3	9.8 7.2	1.5 1.5	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $n\overline{Y}$	1	1.5 1.5	6.6 5.9	11.1 8.3	1.5 1.5	12.7 9.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	4.3 4.2	6.8 6.7	1.5 1.5	7.4 7.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	6.1 5.4	7.8 6.9	1.5 1.5	8.2 7.3	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nI_n, S_n) to Output ($n\overline{Y}$) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11373

Octal D-Type Transparent Latch; 3-State

Product Specification

FEATURES

- **8-bit transparent latch**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11373 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11373 device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (LE) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (LE) input is High. The latch remains

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay D_n to Q_n	C_L = 50pF; V_{CC} = 5V	5.8	7.0	ns
C_{PD}	Power dissipation capacitance per latch[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	47	65	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	36	54	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate; Data inputs	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

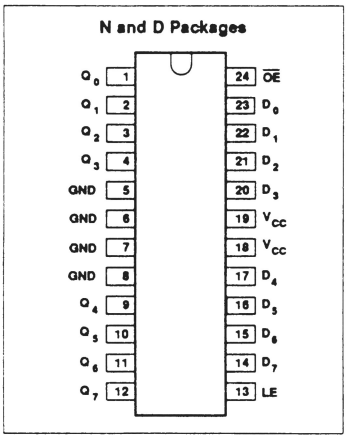
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

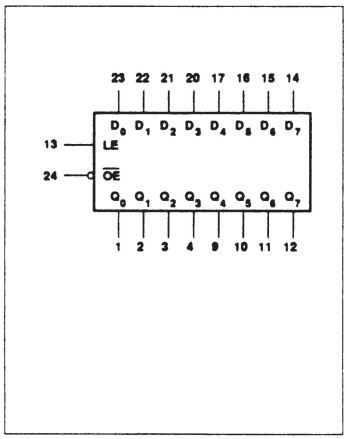
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11373N 74ACT11373N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11373D 74ACT11373D

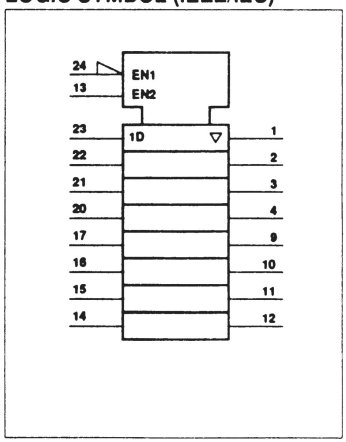
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



transparent to the data inputs while LE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

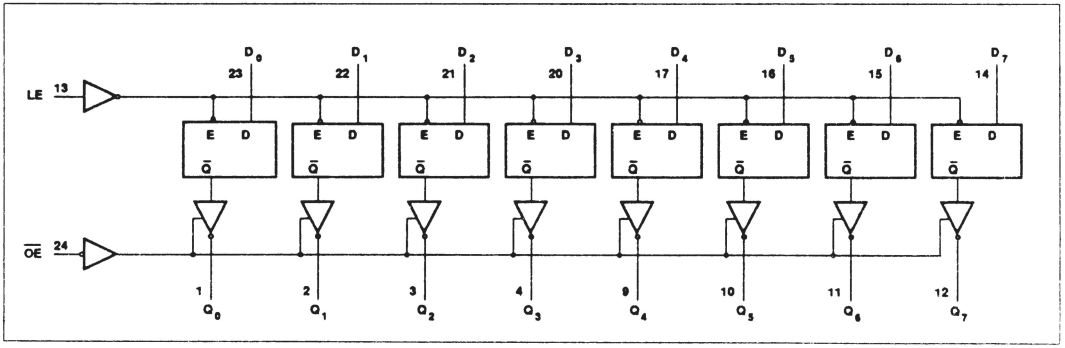
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{OE}$	Output enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	Q_0 - Q_7	Data outputs
13	LE	Latch enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_n
Enable and read register	L L	H H	L H	L H	L H
Latch and read register	L L	↓ ↓	l h	L H	L H
Hold	L	L	X	NC	NC
Disable outputs	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the High-to-Low E transition
X = Don't care
NC = No change
Z = High-impedance "OFF" state
↓ = High-to-Low transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11373			74ACT11373			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]		3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data, E	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11373				74ACT11373				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11373					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	1	1.5 1.5	9.0 8.0	13.1 10.6	1.5 1.5	14.8 11.7	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n	4	1.5 1.5	10.0 9.5	14.5 12.8	1.5 1.5	16.3 14.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.0 8.5	13.1 11.6	1.5 1.5	14.7 13.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.5 7.5	12.0 10.2	1.5 1.5	12.7 10.8	ns
t_W	LE Pulse Width High or Low	4	5.5			5.5		ns
t_S	Setup time D_n to LE↓	3	4.0			4.0		ns
t_H	Hold time D_n to LE↓	3	2.0			2.0		ns

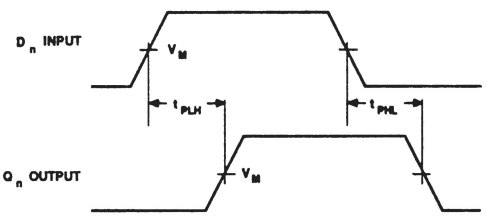
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11373					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	1	1.5 1.5	6.0 5.5	8.9 7.6	1.5 1.5	10.3 8.4	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n	4	1.5 1.5	6.5 6.5	10.0 9.1	1.5 1.5	11.3 10.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.5 6.0	9.5 8.6	1.5 1.5	10.8 9.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	8.5 6.0	10.6 8.2	1.5 1.5	11.1 8.7	ns
t_W	LE Pulse Width High or Low	4	4.0			4.0		ns
t_S	Setup time D_n to LE↓	3	3.5			3.5		ns
t_H	Hold time D_n to LE↓	3	2.0			2.0		ns

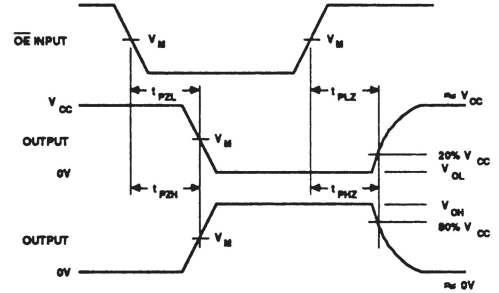
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11373					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	1	1.5 1.5	7.5 6.5	10.3 9.3	1.5 1.5	11.8 10.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n	4	1.5 1.5	8.5 8.5	11.3 10.9	1.5 1.5	13.0 12.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.0 7.5	10.7 10.9	1.5 1.5	12.5 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.0 7.5	12.1 9.5	1.5 1.5	12.5 10.1	ns
t_W	LE Pulse Width High or Low	4	5.0			5.0		ns
t_S	Setup time D_n to LE↓	3	3.5			3.5		ns
t_H	Hold time D_n to LE↓	3	3.5			3.5		ns

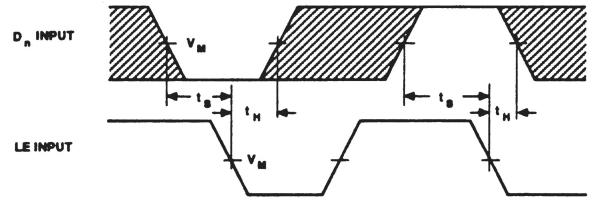
AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (D_n) to Output (Q_n) Propagation Delays

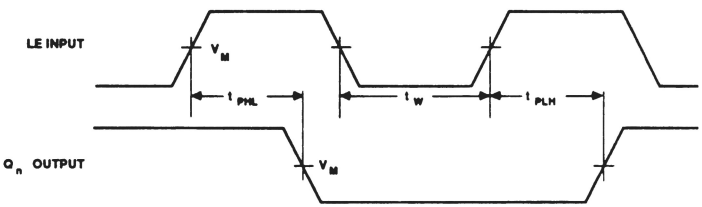


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times



Waveform 3. Waveforms Showing the Data Setup and Hold Times for D_n Input to LE Input

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 4. Waveforms Showing the Latch Enable Input (LE) Pulse Width and the Latch Enable Input to Output (Q_n) Propagation Delays

74AC/ACT11374

Octal D-Type Flip-Flop; Positive-Edge Trigger; 3–State

Product Specification

FEATURES

- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11374 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11374 device is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge-triggered. Once the set-up requirements are met, when the Clock Pulse (CP) rises the state of each D input is transferred to the corresponding flip-flop's Q output.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF; V_{CC} = 5V	6.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	75	107	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	66	96	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate; Data inputs	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.5V	110	70	MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:

   f_I = input frequency in MHz, C_L = output load capacitance in pF,

   f_O = output frequency in MHz, V_{CC} = supply voltage in V,

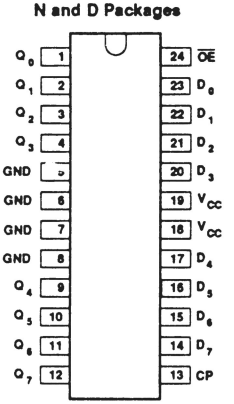
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

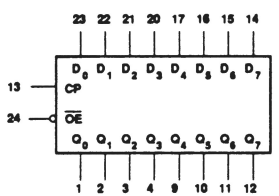
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11374N 74ACT11374N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11374D 74ACT11374D

PIN CONFIGURATION

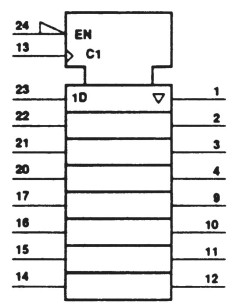
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

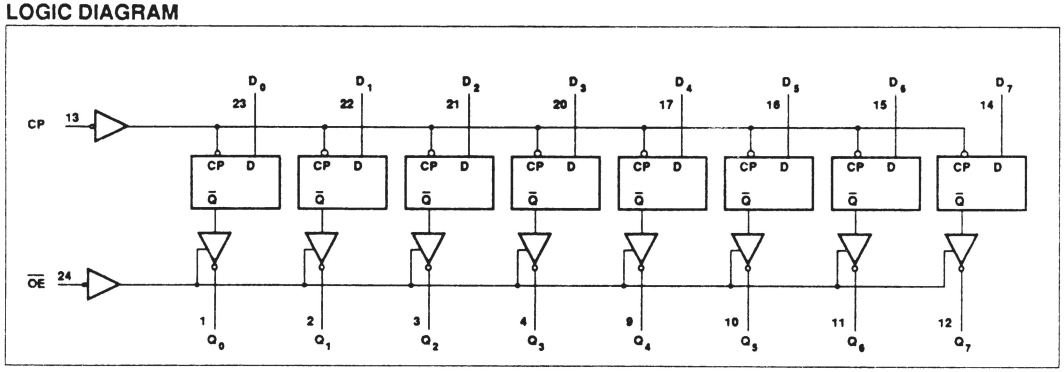
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{OE}$	Output enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	Q_0 - Q_7	Data outputs
13	CP	Clock input
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_n
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Disable outputs	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
Z = High-impedance "OFF" state
↑ = Low-to-High transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11374			74ACT11374			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]		3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11374				74ACT11374				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11374					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	90		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	9.5 9.0	12.5 12.6	1.5 1.5	14.2 14.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.0 8.0	10.9 11.1	1.5 1.5	12.3 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.0 8.0	12.1 10.7	1.5 1.5	12.5 11.6	ns
t_W	Clock pulse width High or Low	3	6.5			6.5		ns
t_S	Setup time D_n to CP	3	2.5			2.5		ns
t_H	Hold time D_n to CP	3	4.5			4.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11374					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	95	110		95		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	6.5 5.5	9.0 9.1	1.5 1.5	10.2 10.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.5 5.5	8.0 8.4	1.5 1.5	9.1 9.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.0 6.0	11.0 8.6	1.5 1.5	11.2 9.2	ns
t_W	Clock pulse width High or Low	3	5.0			5.0		ns
t_S	Setup time D_n to CP	3	2.5			2.5		ns
t_H	Hold time D_n to CP	3	3.5			3.5		ns

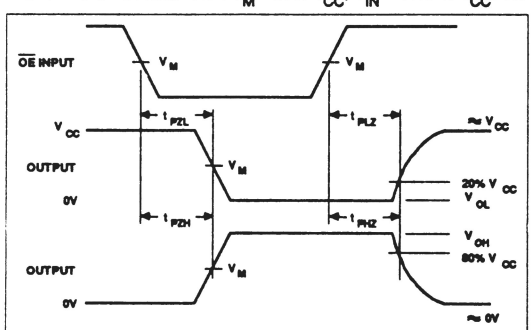
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

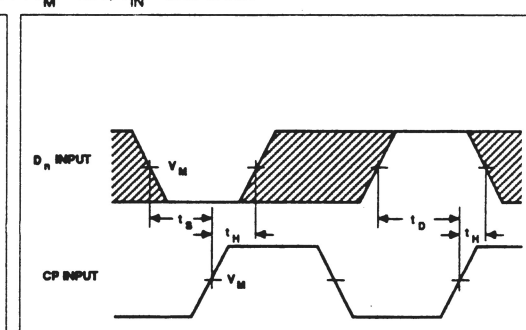
SYMBOL	PARAMETER	WAVEFORM	74ACT11374					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	55	70		55		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	4	1.5 1.5	8.5 8.5	10.7 11.3	1.5 1.5	12.4 13.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.5	11.0 11.0	1.5 1.5	12.3 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	11.0 8.0	12.7 10.0	1.5 1.5	13.2 10.8	ns
t_W	Clock pulse width High or Low	3	9.0			9.0		ns
t_S	Setup time D_n to CP	3	3.0			3.0		ns
t_H	Hold time D_n to CP	3	5.5			5.5		ns

AC WAVEFORMS

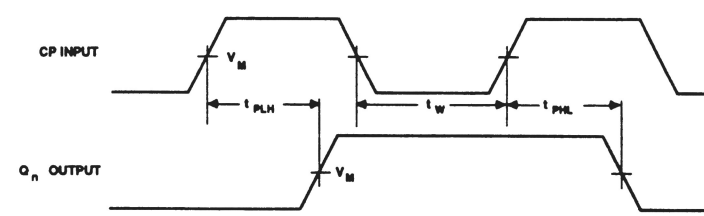
AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the 3-State Output Enable and Disable Times



Waveform 2. Waveforms Showing the Data Set-up and Hold Times for D_n Input to CP Input



Waveform 3. Waveforms Showing the Clock Input (CP) Pulse Width to Output (Q_n) Propagation Delays

74AC/ACT11520

8-Bit Identity Comparator with Input Pull-Up

Preliminary Specification

FEATURES

- **Compares two 8-bit words**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11520 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11520 identity comparators perform comparisons on two 8-bit binary or BCD words and provides a Low output when the two words match bit for bit.

The 74AC/ACT11520 identity comparators also feature 20-k ohm pull-up termination resistors on the Q inputs for analog or switch data and a provision for $\overline{P=Q}$ totem-pole outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay P_n or Q_n to $\overline{P=Q}$	C_L = 50pF; V_{CC} = 5V	5.0		ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	79		pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

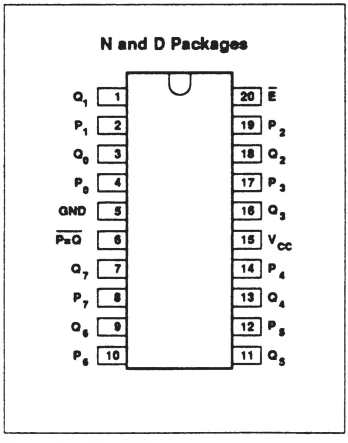
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

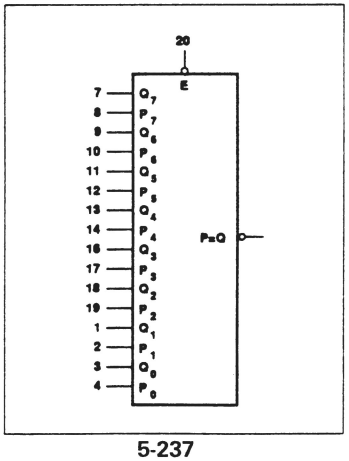
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11520N 74ACT11520N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11520D 74ACT11520D

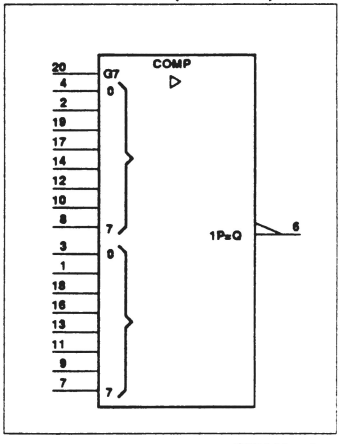
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



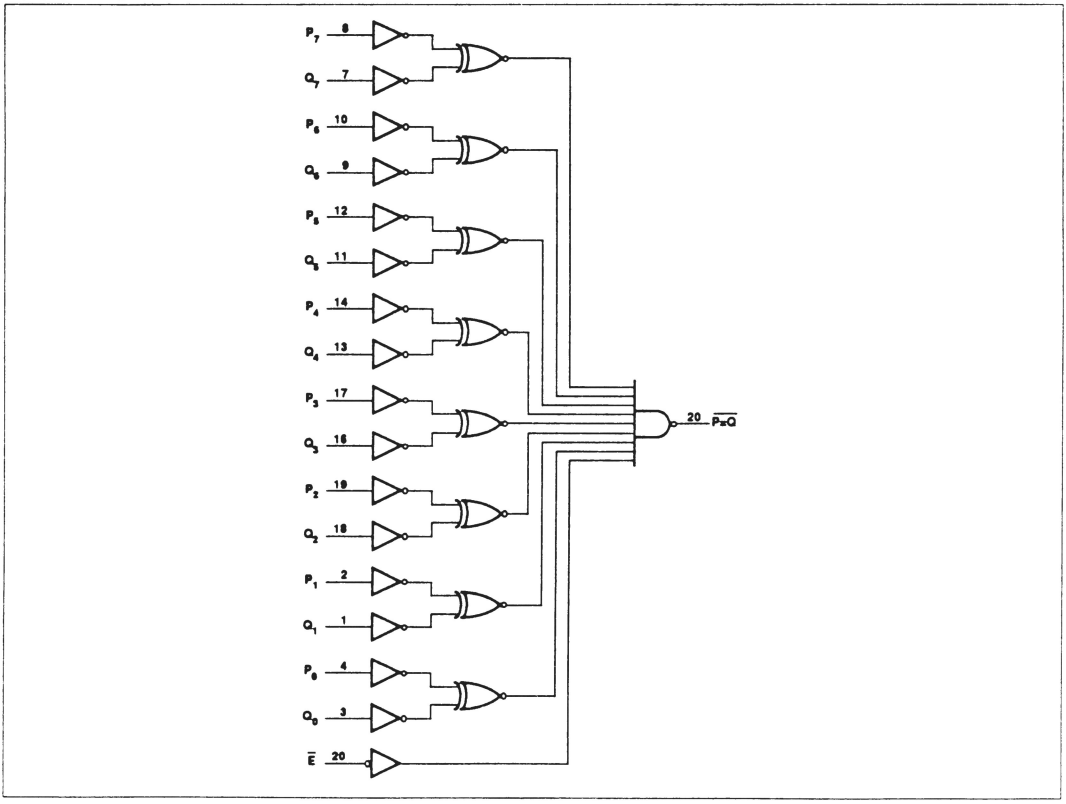
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
4, 2, 19, 17 14, 12, 10, 8	P_0 to P_7	Data inputs
3, 1, 18, 16 13, 11, 9, 7	Q_0 to Q_7	Data inputs
11	$\overline{E}$	Enable input (active Low)
20	$\overline{P=Q}$	Output
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{E}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11520			74ACT11520			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11520				74ACT11520				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11520					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns

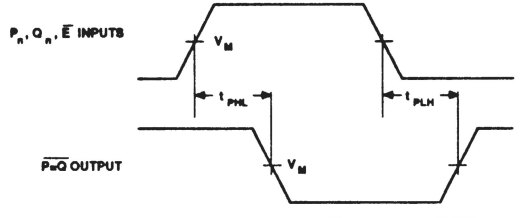
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11520					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11520					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Inputs (P_n, Q_n, $\overline{E}$) to Output ($\overline{P=Q}$) Propagation Delays

74AC/ACT11521

8-Bit Identity Comparator

Preliminary Specification

FEATURES

- **Compares two 8-bit words**
- **Output capability: ±24 mA**
- **Inputs are TTL-voltage compatible**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11521 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11521 identity comparators perform comparisons on two 8-bit binary or BCD words and provides a Low output when the two words match bit for bit.

The 74AC/ACT11521 identity comparators also feature a provision for $\overline{P=Q}$ totem-pole outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay P_n or Q_n to $\overline{P=Q}$	C_L = 50pF; V_{CC} = 5V	5.0		ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	79		pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

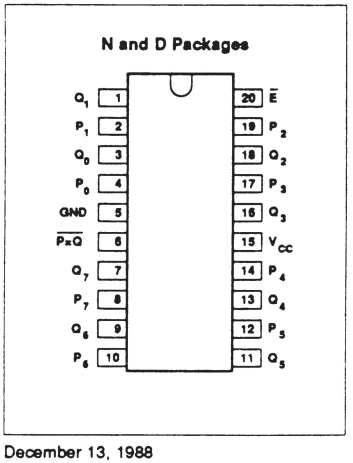
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

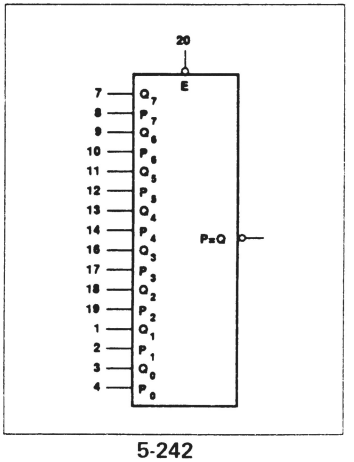
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11521N 74ACT11521N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11521D 74ACT11521D

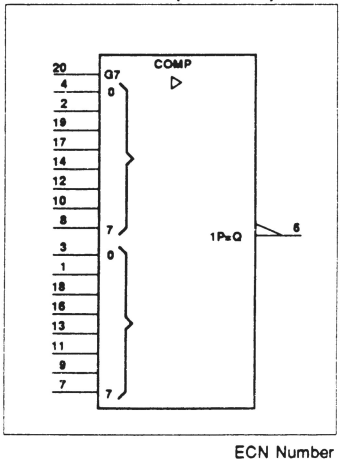
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



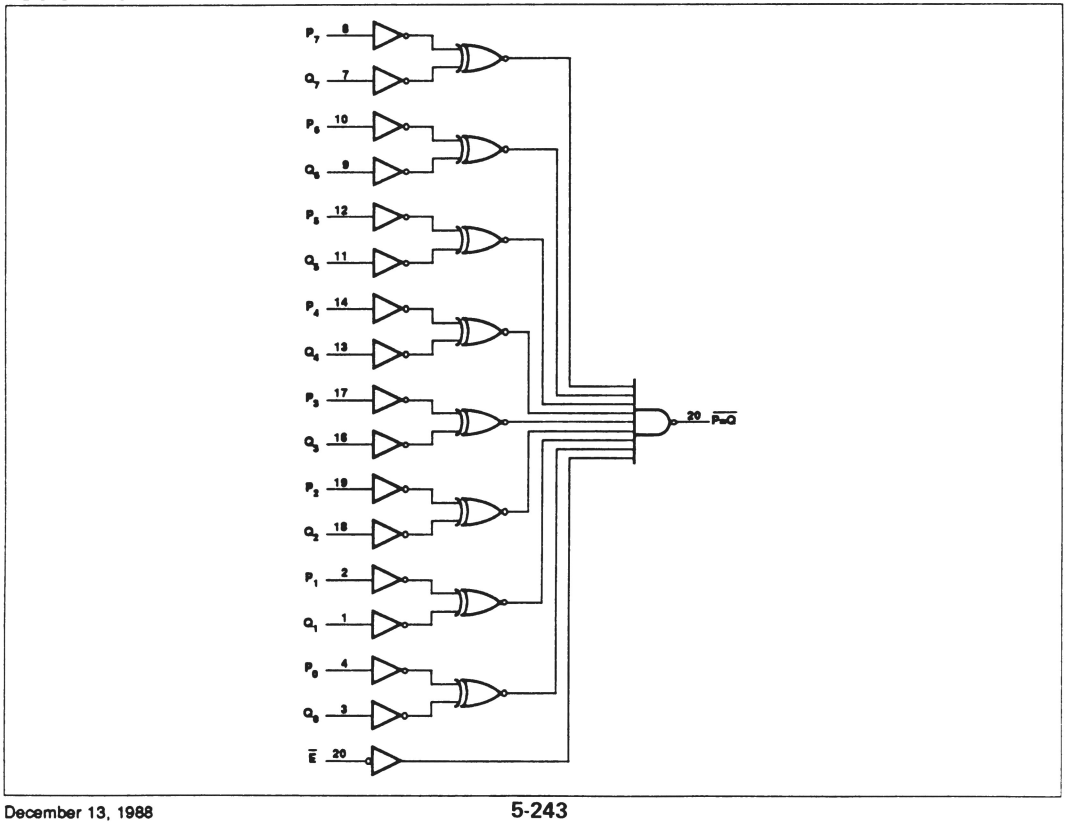
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
4, 2, 19, 17 14, 12, 10, 8	P_0 to P_7	Data inputs
3, 1, 18, 16 13, 11, 9, 7	Q_0 to Q_7	Data inputs
11	$\overline{E}$	Enable input (active Low)
20	$\overline{P=Q}$	Output
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{E}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11521			74ACT11521			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11521				74ACT11521				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11521					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns

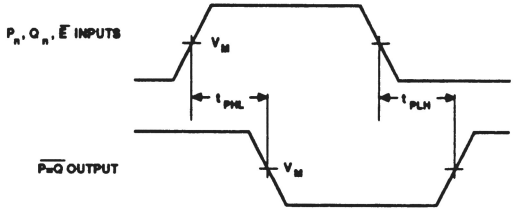
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11521					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11521					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay P_n, Q_n to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Inputs (P_n, Q_n, $\overline{E}$) to Output ($\overline{P=Q}$) Propagation Delays

74AC/ACT11533

Octal D-Type Transparent Latch (3-State), Inverting

Product Specification

FEATURES

- **8-bit transparent latch**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11533 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11533 device is an octal transparent latch coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by Latch Enable (LE) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (LE) input is High. The latch remains

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	C_L = 50pF; V_{CC} = 5V	5.3	6.8	ns
C_{PD}	Power dissipation capacitance per latch[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	55	69	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	44	58	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

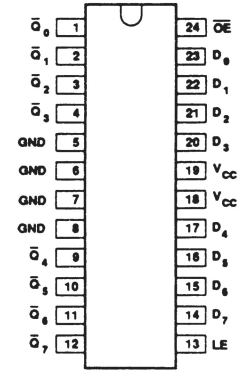
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

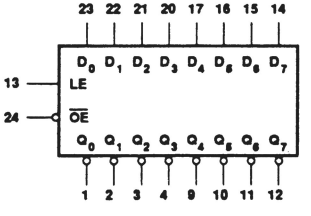
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11533N 74ACT11533N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11533D 74ACT11533D

PIN CONFIGURATION

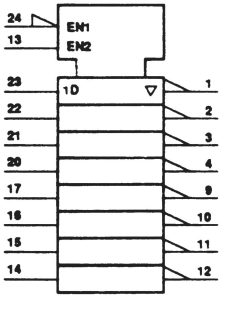
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



transparent to the data inputs while LE is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

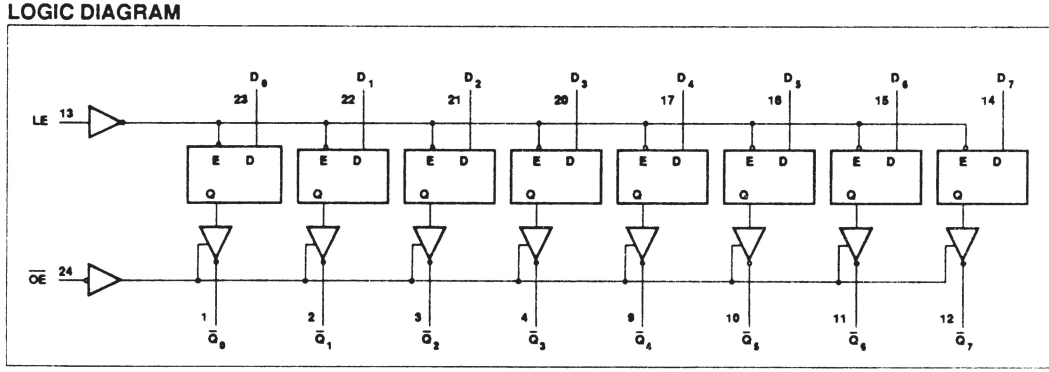
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{OE}$	Output enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs
13	LE	Latch enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	LE	D_n		$\overline{Q}_n$
Enable and read register	L L	H H	L H	L H	H L
Latch and read register	L L	↓ ↓	l h	L H	H L
Hold	L	L	X	NC	NC
Disable outputs	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the High-to-Low E transition
X = Don't care
NC = No change
Z = High-impedance "OFF" state
↓ = High-to-Low transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11533			74ACT11533			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]		3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data, E	0		10	0		10	ns/V
		Output enable	0		10	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11533				74ACT11533				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11533					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	1	1.5 1.5	8.5 7.5	12.6 10.1	1.5 1.5	14.3 11.3	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}_n$	4	1.5 1.5	10.0 9.5	14.5 12.8	1.5 1.5	16.5 14.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.0 8.5	13.1 11.6	1.5 1.5	14.7 13.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.5 7.5	12.0 10.2	1.5 1.5	12.8 11.0	ns
t_W	LE Pulse Width High or Low	4	5.5			5.5		ns
t_S	Setup time D_n to LE↓	3	4.0			4.0		ns
t_H	Hold time D_n to LE↓	3	2.0			2.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11533					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	1	1.5 1.5	5.5 5.0	8.4 7.1	1.5 1.5	9.8 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}_n$	4	1.5 1.5	6.5 6.5	10.0 9.1	1.5 1.5	11.3 10.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.5 6.0	9.5 8.6	1.5 1.5	10.8 9.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	8.5 6.0	10.7 8.2	1.5 1.5	11.4 8.9	ns
t_W	LE Pulse Width High or Low	4	4.0			4.0		ns
t_S	Setup time D_n to LE↓	3	3.5			3.5		ns
t_H	Hold time D_n to LE↓	3	2.0			2.0		ns

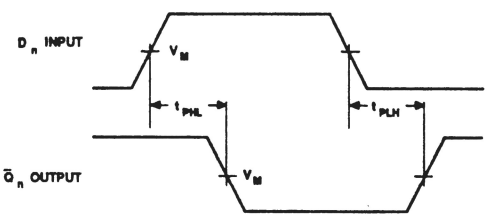
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

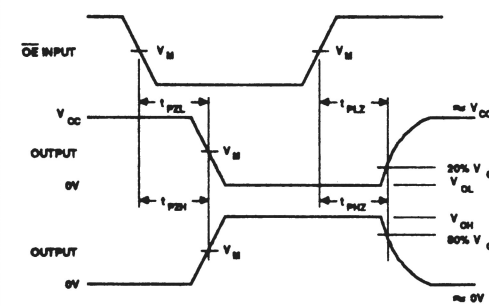
SYMBOL	PARAMETER	WAVEFORM	74ACT11533					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{O}_n$	1	1.5 1.5	7.0 6.5	10.1 8.4	1.5 1.5	11.3 9.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{O}_n$	4	1.5 1.5	8.5 8.5	11.3 10.7	1.5 1.5	13.0 12.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.5	10.7 10.9	1.5 1.5	12.5 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.5 7.5	12.1 9.5	1.5 1.5	12.8 10.3	ns
t_W	LE Pulse Width High or Low	4	5.0			5.0		ns
t_S	Setup time D_n to LE↓	3	3.5			3.5		ns
t_H	Hold time D_n to LE↓	3	3.5			3.5		ns

AC WAVEFORMS

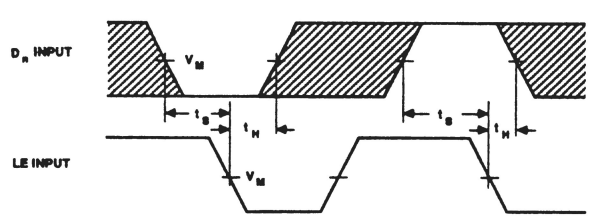
AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (D_n) to Output ($\overline{O}_n$) Propagation Delays

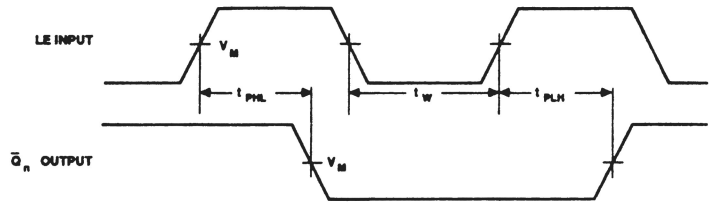


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times



Waveform 3. Waveforms Showing the Data Setup and Hold Times for D_n Input to LE Input

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 4. Waveforms Showing the Latch Enable Input (LE) Pulse Width and the Latch Enable Input to Output ($\overline{O}_n$) Propagation Delays

74AC/ACT11534

Octal D-Type Flip-Flop; Positive-Edge Trigger (3-State), Inverting

Product Specification

FEATURES

- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11534 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11534 device is an 8-bit, edge-triggered register coupled to eight 3-State, inverting output buffers. The two sections of the device are controlled independently by Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge-triggered. Once the set-up requirements are met, when the Clock Pulse (CP) rises the state of each D input is transferred to the corresponding flip-flop's $\overline{Q}$ output.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to $\overline{Q}_n$	C_L = 50pF; V_{CC} = 5V	7.0	8.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled	75	92	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled	65	82	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate; Data inputs	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.5V	100	70	MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:

   f_I = input frequency in MHz, C_L = output load capacitance in pF,

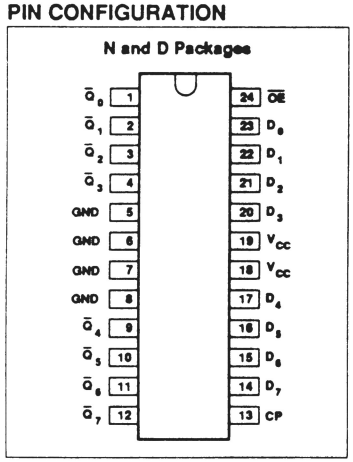
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,

   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

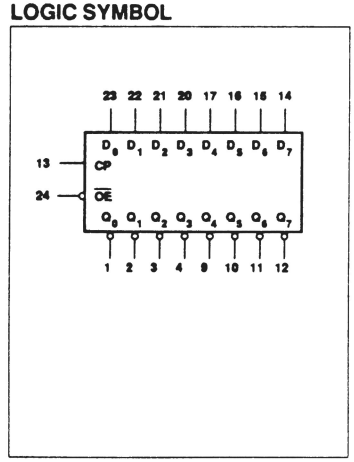
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11534N 74ACT11534N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11534D 74ACT11534D

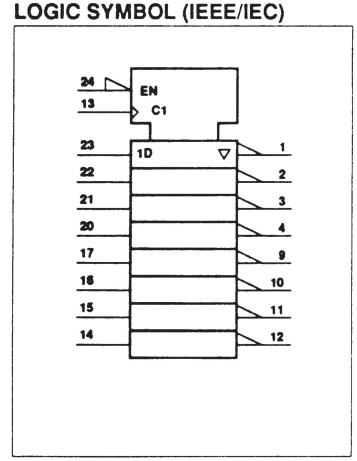
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal D-Type Flip-Flop; Positive-Edge Trigger (3-State), Inverting

74AC/ACT11534

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State inverting buffers independent of the latch operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

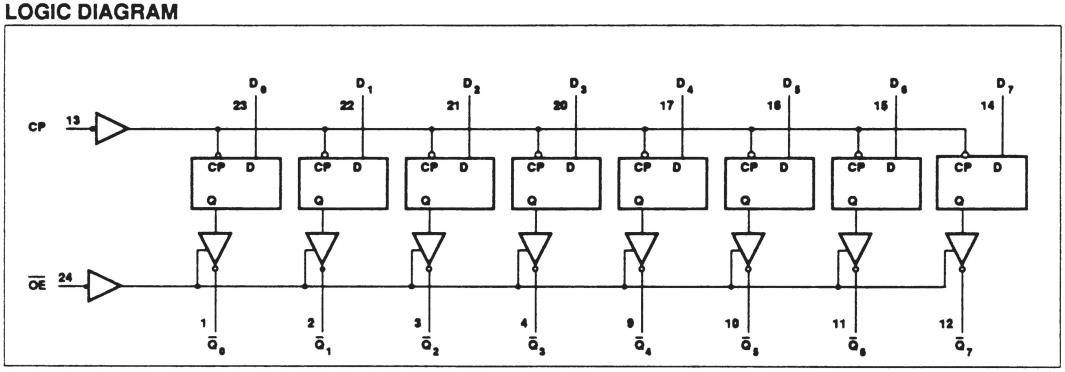
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{OE}$	Output enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}_0$ - $\overline{Q}_7$	Data outputs
13	CP	Clock input
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{Q}_n$
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Disable outputs	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
Z = High-impedance "OFF" state
↑ = Low-to-High transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11534			74ACT11534			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]		3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11534				74ACT11534				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11534					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	50	75		50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{O}_n$	1	1.5 1.5	11.0 11.0	15.3 15.7	1.5 1.5	17.6 17.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.0 9.0	12.8 12.6	1.5 1.5	14.6 14.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	10.0 8.0	12.6 13.0	1.5 1.5	13.3 13.8	ns
t_W	Clock pulse width High or Low	3	10.0			10.0		ns
t_S	Setup time D_n to CP	3	3.5			3.5		ns
t_H	Hold time D_n to CP	3	5.5			5.5		ns

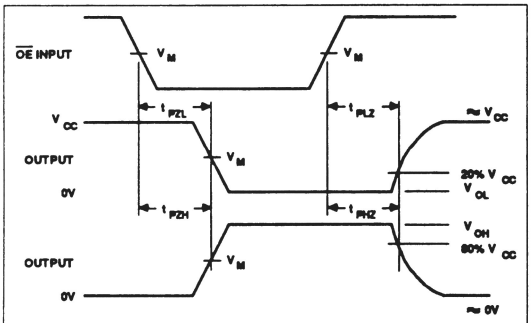
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11534					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	100		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{O}_n$	1	1.5 1.5	7.0 7.0	10.3 10.7	1.5 1.5	11.7 12.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	6.0 6.0	9.2 9.2	1.5 1.5	10.4 10.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.0 6.0	11.1 8.8	1.5 1.5	11.6 9.2	ns
t_W	Clock pulse width High or Low	3	6.5			6.5		ns
t_S	Setup time D_n to CP	3	3.5			3.5		ns
t_H	Hold time D_n to CP	3	4.5			4.5		ns

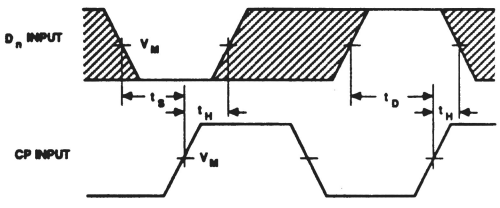
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11534					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	55	70		55		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	4	1.5 1.5	8.5 8.5	12.7 13.3	1.5 1.5	14.5 15.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.5 7.5	12.0 12.2	1.5 1.5	13.3 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	11.0 8.0	12.9 11.2	1.5 1.5	13.5 12.0	ns
t_W	Clock pulse width High or Low	3	9.0			9.0		ns
t_S	Setup time D_n to CP	3	3.0			3.0		ns
t_H	Hold time D_n to CP	3	5.5			5.5		ns

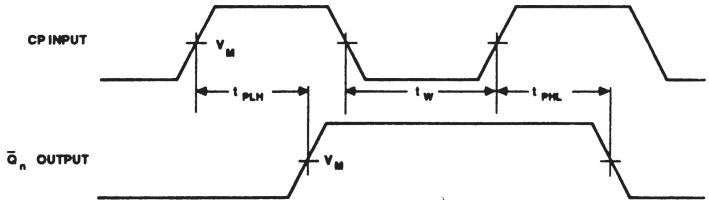
AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}; ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the 3-State Output Enable and Disable Times



Waveform 2. Waveforms Showing the Data Set-up and Hold Times for D_n Input to CP Input



Waveform 3. Waveforms Showing the Clock Input (CP) Pulse Width to Output ($\overline{Q}_n$) Propagation Delays

Signetics

74AC/ACT11640

Octal Transceiver w/Direction Pin; 3-State; INV

Product Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffers**
- **Inverting version of '245**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11640 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11640 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V		6.0	ns
C_{PD}	Power dissipation capacitance per buffer[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Enabled		47	pF
		V_{CC} = 5.0V; f = 1MHz; C_L = 50pF; Disabled		12	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
C_{IO}	I/O capacitance	V_I = 0V or V_{CC}	12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

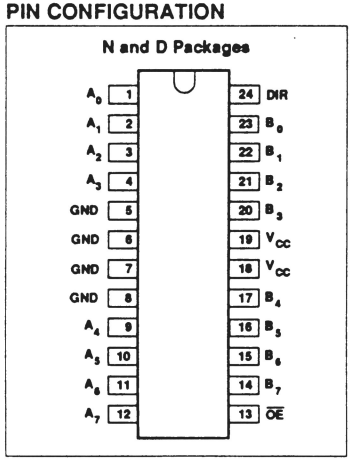
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

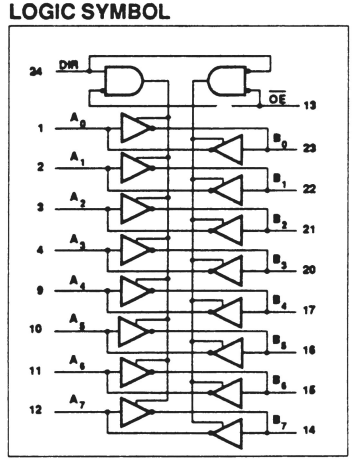
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11640N 74ACT11640N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11640D 74ACT11640D

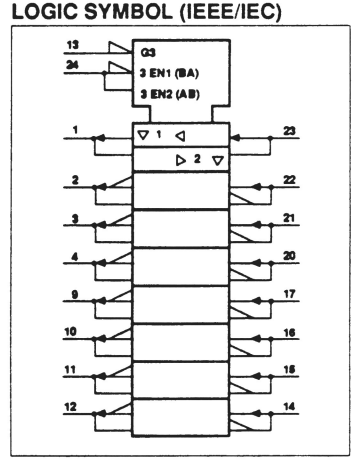
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	DIR	Direction control input
1, 2, 3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
13	$\overline{OE}$	Output enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	$A = \overline{B}$	inputs
L	H	inputs	$B = \overline{A}$
H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11640			74ACT11640			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50-	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11640				74ACT11640				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}; V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11640					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5			1.5 1.5		ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5			1.5 1.5		ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5			1.5 1.5		ns

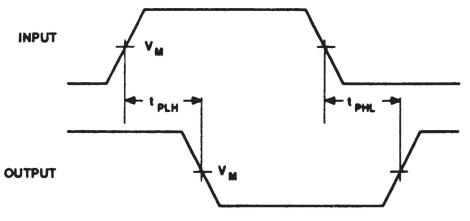
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11640					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5			1.5 1.5		ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5			1.5 1.5		ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5			1.5 1.5		ns

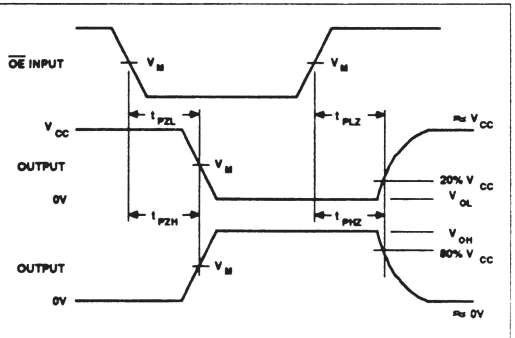
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11640					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	1	1.5 1.5	6.3 5.7	9.6 8.6	1.5 1.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.8 8.4	12.2 12.3	1.5 1.5	13.4 13.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.1 9.6	12.9 13.1	1.5 1.5	13.9 14.2	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}; V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input to Output Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

74AC/ACT11810

Quad 2-Input Exclusive-NOR Gate

Preliminary Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11810 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11810 provides four separate 2-input exclusive-NOR gate functions.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF; V_{CC} = 5V	4.5	5.6	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	24	26	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V

Note:

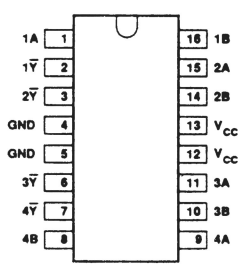
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

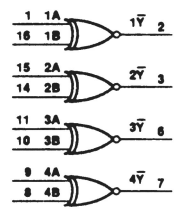
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11810N 74ACT11810N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11810D 74ACT11810D

PIN CONFIGURATION

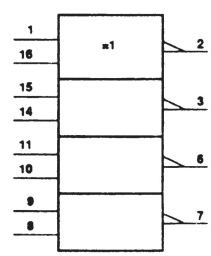
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	$n\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11810			74ACT11810			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11810				74ACT11810				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11810					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	5.9 5.3	7.9 6.7	1.5 1.5	8.6 7.4	ns

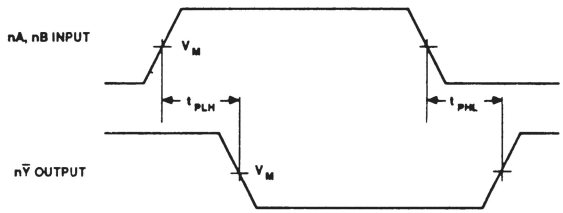
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11810					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	4.5 4.4	6.2 5.7	1.5 1.5	6.7 6.2	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_R = t_F$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11810					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5	5.6 5.6	7.2 7.1	1.5 1.5	7.8 7.7	ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 1. Waveforms Showing the Input (nA, nB) to Output (n$\overline{Y}$) Propagation Delays

74AC/ACT11898

10-Bit Serial-In Parallel-Out Shift Register

Preliminary Specification

FEATURES

- **Gated serial data inputs**
- **Fully buffered clock and data inputs**
- **Fully synchronous data transfers**
- **Typical shift frequency of 100MHz**
- **Asynchronous master reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11898 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11898 10-bit Serial-In Parallel-Out Shift Register is an edge-triggered shift register with serial data entry and an output from each of the 10 stages. Data is entered serially through one of two inputs (A • B); either input can be used as an active-High enable for data entry through the other input. Otherwise

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n ($\overline{MR}$ = High)	C_L = 50pF; V_{CC} = 5V	7.0	7.6	ns
C_{PD}	Power dissipation capacitance per gate[1]	V_{CC} = 5.0V; f = 1MHz; C_L = 50pF	121	117	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
$\Delta t/\Delta v$	Maximum input rise or fall rate	C_L = 50pF; V_{CC} = 5.5V	10	10	ns/V
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.0V	100	90	MHz

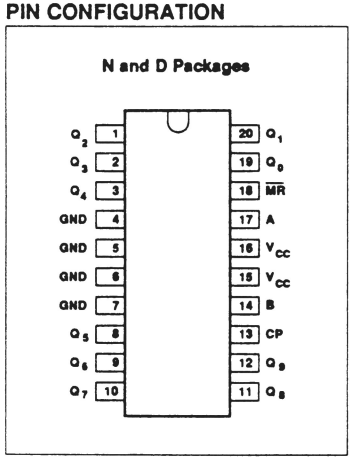
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

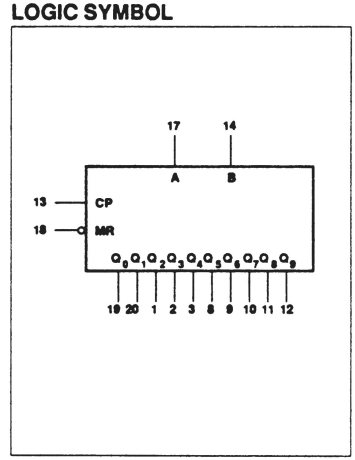
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11898N 74ACT11898N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11898D 74ACT11898D

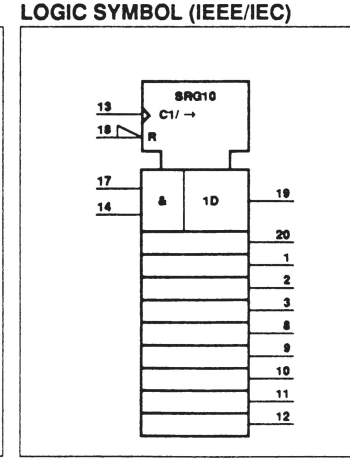
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



both inputs must be connected to the input data or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input and enters the logical AND of the two inputs (A • B) that existed one setup time before the rising clock edge into Q_0.

A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

PIN DESCRIPTION

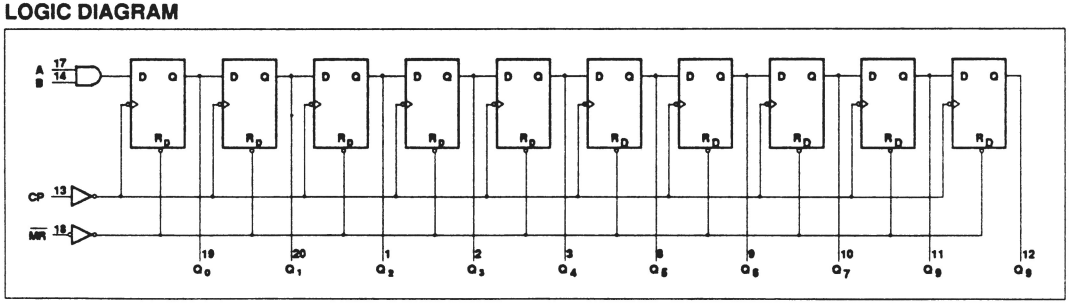
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18	$\overline{MR}$	Asynchronous master reset (active Low)
13	CP	Clock input (Low-to-High, edge-triggered)
17, 14	A, B	Data inputs
19, 20, 1, 2, 3, 8, 9, 10, 11, 12	Q_0 - Q_9	Parallel outputs outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	A	B	Q_0	Q_1	—	Q_9
Reset (clear)	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_9
	H	↑	l	h	L	q_0	—	q_9
	H	↑	h	l	L	q_0	—	q_9
	H	↑	h	h	H	q_0	—	q_9

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q_n = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11898			74ACT11898			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage[1]	3.0	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11898				74ACT11898				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11898					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	60	70		60		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	8.9 8.8	10.8 10.7	1.5 1.5	11.8 11.6	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	9.6	11.5	1.5	12.6	ns
t_S	Setup time, High or Low A, B to CP	3	13.5			13.5		ns
t_H	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t_W	Clock pulse width (shift) High or Low	1	8.0			8.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	3.0			3.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

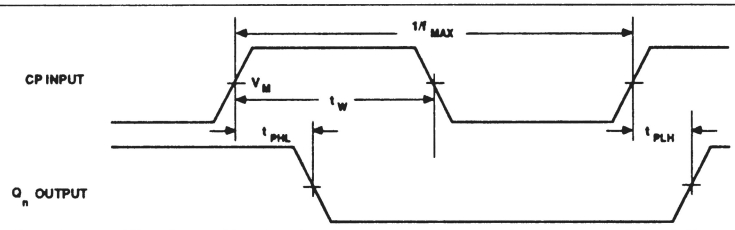
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74AC11898					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	100		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	6.4 6.8	8.0 8.4	1.5 1.5	8.8 9.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	7.2	8.9	1.5	9.6	ns
t_S	Setup time, High or Low A, B to CP	3	8.5			9.5		ns
t_H	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t_W	Clock pulse width (shift) High or Low	1	5.5			5.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	2.5			2.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

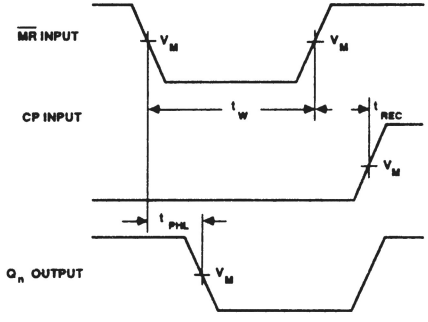
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V GND = 0V; $t_r = t_f$ = 3ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	74ACT11898					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	80	90		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.5 1.5	7.5 7.7	9.0 9.1	1.5 1.5	9.8 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	9.5	11.0	1.5	11.9	ns
t_S	Setup time, High or Low A, B to CP	3	9.5			9.5		ns
t_H	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t_W	Clock pulse width (shift) High or Low	1	6.0			6.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V

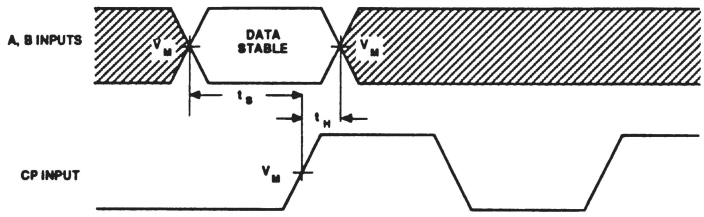


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Q_n) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

AC WAVEFORMS AC : V_M = 50% V_{CC}, V_{IN} = GND to V_{CC}. ACT : V_M = 1.5V, V_{IN} = GND to 3.0V (Continued)



Waveform 4. Waveforms Showing the Data Set-up and Hold Times for the InputS (A,B)

Section 6
Application Notes

INDEX

AN600 Handling Precautions 6-3
AN601 Simultaneous Switching Evaluation of Advanced CMOS Logic 6-5
AN203 Test Fixtures for High-Speed Logic 6-9

AN600
Handling Precautions

Application Note

ELECTROSTATIC CHARGES

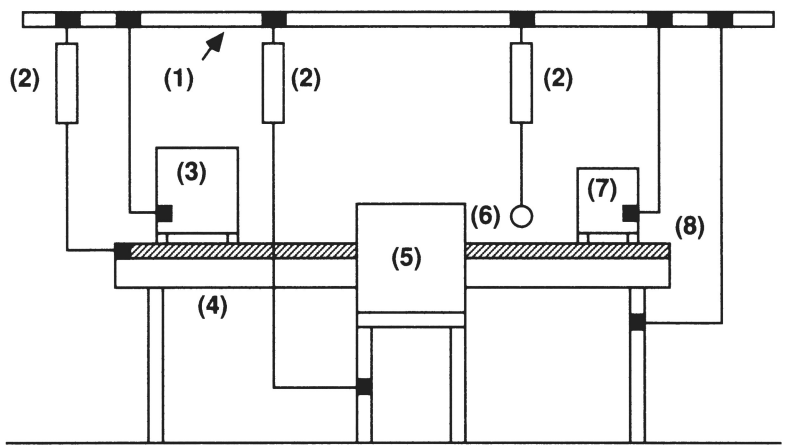
Electrostatic charges can be stored in many things; for example, man-made fiber clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depends on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our CMOS ICs are internally protected against electrostatic discharge, but they can be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safety handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is 1kΩ to 0.5MΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work-bench should be grounded via a wrist strap and a resistor.
- All electrical equipment should be connected to the mains via a ground-leakage switch and the equipment cases should be grounded.
- Relative humidity should be maintained between 50% and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.



NOTES:

1. Grounding rail
2. Resistor (500kΩ ±10%, 0.5W)
3. Ionizer
4. Work bench
5. Chair
6. Wrist strap
7. Electrical equipment
8. Conductive surface/antistatic sheet

Figure 1. Protected Work Station

RECEIPT AND STORAGE

CMOS ICs are packed for dispatch in antistatic/conductive boxes, rails or blister tape. The fact that the ICs are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The ICs should be kept in their original packing while in storage. If a bulk container is partially unpacked, the tasks should be performed at a protected work station. Any CMOS ICs that are temporarily stored should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

CMOS ICs must be removed from their protective packing with grounded component-pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more ICs from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the CMOS ICs are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand-tools should be of conductive or antistatic material and, where possible, not insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Handle assembled circuit boards containing CMOS ICs in the same way as unmounted CMOS ICs. They should also carry warning labels and be packed in conductive or antistatic packing.

AN601
Simultaneous Switching Evaluation of Advanced CMOS Logic

Application Note

INTRODUCTION

The purpose of this paper is to define what Simultaneous Switching Evaluation (SSE) is, why it is tested, and how it is tested for the Advanced CMOS Logic (ACL) family of integrated circuits.

WHY SHOULD SSE BE PERFORMED

The purpose of SSE is to evaluate what effect switching more than one output simultaneously has on the performance of the circuit. SSE becomes important in any high-performance line of circuits because the propagation delays and output edge rates are very fast.

Fast edge rates can team up with parasitic inductances to produce unwanted side effects such as output disturbances and/or performance degradations. Output disturbances can manifest themselves in the form of glitches or bumps from solid low levels near or above the low threshold of a subsequent device, or from solid highs down near or below the high threshold of a subsequent device. Degradations take the form of slowed propagation delays, abnormally slow or distorted output edges, or lost data in devices containing memory. Any and all of these unwanted side effects will cause a system to perform unpredictably and unreliably. Output disturbances especially can be the cause of a multitude of system performance abnormalities.

Since ACL is considered to be a high-performance family of circuits, SSE is necessary in order to insure that the circuits will perform as specified under any switching condition. To guarantee that ACL will perform satisfactorily under multiple output switching conditions, comprehensive SSE is performed prior to product release. Tests are done to evaluate the magnitude of output disturbances, the integrity of stored data, and the propagation delays and output transition times under conditions of multiple outputs switching.

Each of these evaluations will now be explained and a very general procedure for measuring each will be given. For a specific step-by-step procedure for measuring each, including fixturing and equipment requirements, refer to Appendix 1.

OUTPUT DISTURBANCE TESTS

The purpose of these tests is to determine the magnitude of disturbances on the High and Low level of the outputs when multiple outputs are switching. The terms V_{OHV} and V_{OLP} are used to describe the level of these disturbances. V_{OHV} refers to the minimum 'valley' High level output voltage and V_{OLP} refers to the maximum 'peak' Low level output voltage. Figure 1 shows a typical example of what the output disturbances look like and also defines the points where V_{OLP} and V_{OHV} are measured.

For circuits with a single output or a single complementary output, the circuit is set up so that the pin under test is switching and the disturbance levels are then measured at the points on the waveform as shown in Figure 1. For all other circuits, the circuit is set up so that the pin under test is not switching while the other outputs are switching and the disturbance levels are then measured as shown in Figure 1.

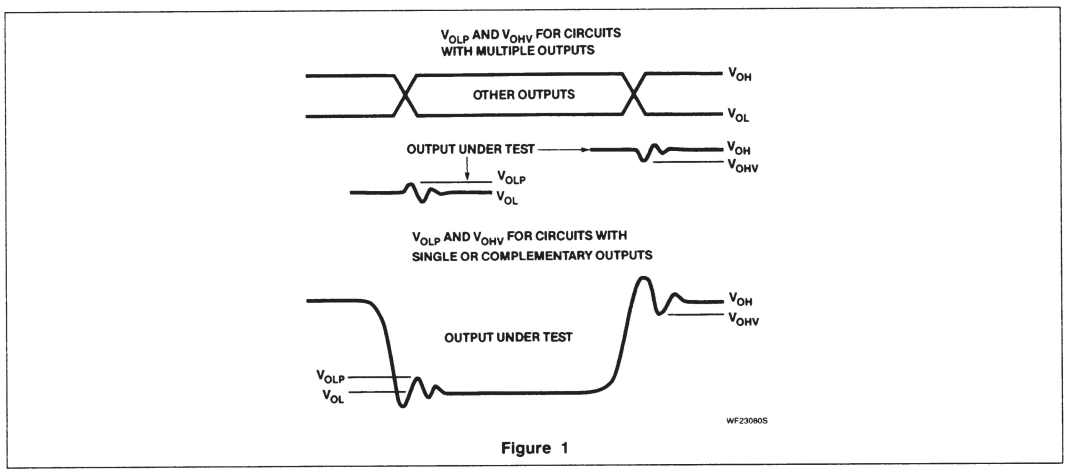


Figure 1

Simultaneous Switching Evaluation of Advanced CMOS Logic

Output High Disturbance

For circuits with a single output or a single complimentary output, set the input conditions so the output(s) under test is switching. For all other circuits, set the input conditions so the output under test is High with as many other outputs as possible switching.

Examine the waveform and record the level of V_{OHV} with respect to V_{CC} as defined by Figure 1.

Output Low Disturbance

For circuits with a single output or a single complimentary output, set the input conditions so the output under test is switching. For all other circuits, set the input conditions so the output under test is Low with as many other outputs as possible switching.

Examine the waveform and record the level of V_{OLP} with respect to Ground as defined by Figure 1.

STORED DATA INTEGRITY

The purpose of this test is to determine what effect, if any, switching multiple outputs simultaneously has on integrity of data storage for circuits with internal storage elements. This test is necessary to insure that the contents of internal storage elements are never corrupted by voltage transients which appear not only on outputs, but also on internal chip supply lines. To perform this test:

- Store a logic 1 in an internal storage element.
- Switch all remaining outputs or, if possible, all outputs.
- Discontinue switching and set input conditions so that the contents of the internal storage elements can be observed.
- Verify that the internal storage element has not changed state.
- Store a logic 0 in an internal storage element and repeat the previous three steps.

SIMULTANEOUS SWITCHING INFLUENCE ON AC PARAMETERS

The purpose of these tests is to determine what effect switching multiple outputs simultaneously has on the propagation delays and output transition times of a circuit. This test is necessary to insure that the propagation delays and output transition times are not significantly degraded by switching multiple outputs simultaneously. To perform these tests:

- Set the input conditions so that the output under test will be switching in the manner required for measurement of the desired propagation delay or output transit on time.
- Switch as many other outputs as possible.
- Measure the propagation delay or output transition time on the output under test using any accurate method.

SUMMARY

The user of ACL circuits should be aware of any potential disturbances or performance degradations that can occur under conditions of multiple output switching and should understand the terms used to describe and measure these. This paper is an attempt to standardize a procedure to which all ACL circuits should be subjected. This method, when followed, will give a user a clear indication of actual device performance.

Simultaneous Switching Evaluation of Advanced CMOS Logic

APPENDIX 1
A Step-by-Step Procedure for Evaluating SSE in the Laboratory

1.0 PURPOSE AND SCOPE OF DOCUMENT

1.1 Introduction
This document gives the steps and procedures needed for completing SSE for ACL devices. Testing is done to determine the effects that switching more than one output simultaneously has on output disturbances, stored data integrity, propagation delays, and output transition times.

2.0 EQUIPMENT REQUIREMENTS

2.1 Hardware

Bench Controller	HP9836C or equivalent
Programmable Oscilloscope	TEK7854 or equivalent
Programmable Pulse Generator	HP8161A or EH2000
Temperature Controller	TP412 or equivalent
Power Supply Programmer	ICS4871 or equivalent
Test Fixture	Acceptable high frequency PC board fixture
Plotter	HP7475A or equivalent
Printer	HP2673A or equivalent
Dice System (An optional data generator/analyzer)	HP8180A, HP8182A, and HP15414A

3.0 TEST PROCEDURES FOR TESTS REQUIRING PLOTS

3.1 General
3.1.1 When applicable, plots should be taken on at least one part and data values should be taken on three parts. The one part used for plots should have typical characteristics for the sample as a whole.

3.1.2 The test fixture will be the same one used for standard AC testing. This is a high-frequency PC board fixture featuring adequate grounding and V_{CC} decoupling as well as 50Ω micro strip line for all signal paths and close proximity loading. The test fixture should have V_{CC} decoupling of at least 100μF, 0.1μF, 0.01μF, and 100pF. For a complete discussion of fixturing requirements including grounding, bypassing, and general high-frequency testing requirements refer to the Application Note entitled "Testing and Specifying ACL Logic."

3.1.3 Pulse Generator Setup

For 74AC11XXX	V_{IH} = (0.8 V_{CC}), V_{IL} = (0.2 V_{CC})
For 74ACT11XXX	V_{IH} = 1.5V, V_{IL} = 0.5V
t_R/t_F = 3.0ns	(10 to 90%)
f = 5MHz	
Duty Cycle = 50%	

The input signal should be terminated with 50Ω and then branched out *equally* to all inputs needing the input signal. ("Simultaneous" is defined as the input pin's Simultaneous Logic of the device seeing a given signal at the same moment in time.) Line lengths from the termination to the device pin should be kept as short as possible. The dice system can be used if more flexibility of input programming is necessary. If the dice system is used, interchannel delay between the various channels must be nulled out at the pins of the device. If a gang-type configuration is used to tie the input signal to more than one input, input edge rates should be as close as possible to the 3.0ns times.

3.1.4 All outputs should be loaded with the standard 50pF, 500Ω AC load.

3.1.5 The output to be evaluated should be the one farthest away from the V_{CC} pins. If there are two equidistant outputs, record data on both outputs and plot only the worst-case output. Also, if more than one mode/path exists, all should be checked, but only the worst case tested.

3.2 Output High Disturbance
Measure the V_{OHV} level on an output held High during simultaneous switching.

3.2.1 V_{CC} = −5.5V, Temp. = 55°C and V_{CC} = 5.0V, Temp. = 25°C

3.2.2 Number of devices = 3. Plots should be taken on one part.

3.2.3 Input conditions should be set so that the output under test is High.

3.2.4 Switch the remaining outputs simultaneously from Low to High and record V_{OHV}.

3.2.5 Plot waveforms of a switching input, the High output, and a switching output.

3.2.6 Repeat steps 3.2.4 through 3.2.5 for the following other transitions:

High to Low	
3-State to Low	(If possible)
Low to 3-State	(If possible)
High to 3-State	(If possible)
3-State to High	(If possible)

3.3 Output Low Disturbance Testing

Measure the V_{OLP} level on an output held Low during simultaneous switching.

3.3.1 V_{CC} = 5.5V, Temp. = −55°C and V_{CC} = 5.0V, Temp. = 25°C

3.3.2 Number of devices = 3. Plots should be taken on one part.

3.3.3 Input conditions should be set so that the output under test is Low.

3.3.4 Switch the remaining outputs simultaneously from High to Low and record V_{OLP}.

3.3.5 Plot waveforms of a switching input, the Low output, and a switching output.

3.3.6 Repeat steps 3.3.4 through 3.3.6 for the following other transitons

Low to High	
3-State to Low	(If possible)
Low to 3-State	(If possible)
High to 3-State	(If possible)
3-State to High	(If possible)

3.4 Stored Data Integrity

For devices with internal storage elements, perform tests to insure that internal storage elements aren't corrupted by simultaneous switching of outputs.

3.4.1 V_{CC} = 5.5V, Temp. = −55°C and V_{CC} = 5.0V, Temp. = 25°C

3.4.2 Number of devices = 3.

3.4.3 Store data (both High and Low) in an internal storage element. This can be the same element of the output tested in 3.2 and 3.3.

3.4.4 Switch the remaining outputs simultaneously as was done in 3.2 and 3.3 (including 3-States if possible). Check to see that data is not corrupted with any of the switching.

3.4.5 When possible, the dice system should be utilized to functionally check out various combinations of switching with respect to the above procedures.

3.5 Input Waveform Phase Effects

Check phase effects and measure the delay offset that causes the largest magnitude of output disturbances (when possible).

3.5.1 V_{CC} = 5.5V

3.5.2 Temp. = 25°C and −55°C

3.5.3 Number of devices = 3. Plots should be taken on one part.

3.5.4 Testing is completed by switching half of the outputs 180° out-of-phase from the other half of the outputs.

3.5.5 Adjust the delay on half of the outputs (with respect to the other half) until the worst-case output disturbance is obtained.

3.5.6 Record the edge offset and disturbance magnitudes for three parts.

3.5.7 Plot waveforms (one part) of a switching input from one half and another from the other half with outputs from both halves.

3.5.8 Repeat steps 3.5.5 through 3.5.7 for in-phase effects as well.

4.0 TEST PROCEDURES FOR t_{PD} VS SIMULTANEOUS SWITCHING

4.1 General

Measure propagation delays and output transition times under conditions of multiple outputs switching.

4.1.1 Number of devices = 3

4.1.2 V_{CC} = 5.0V, Temp. = 25°C

4.1.3 Number of outputs tested = 1

4.1.4 Number of outputs switching = 1 to N (when possible)

4.1.5 The test output should be tested for all possible propagation delays (t_{PLH}, t_{PHL}, t_{PZL}, t_{PLZ}, t_{PLH}, and t_{PHZ}) and also transition times (ttlh and tthl) for all conditions of outputs simultaneously switching (1 to n).

4.1.6 All tests should be made with other outputs switching in-phase and then out-of-phase.

AN203
Test Fixtures for High-Speed Logic

Application Note

INTRODUCTION

The Signetics Standard Products Division (SPD) operates a Characterization Laboratory in Orem, Utah. This Lab maintains the capability of testing the 11 logic product families the Division supports. These include: AuTTL-74XXX, Schottky-74SXXX, Low-Power Schottky-74LSXXX, FAST-74FXXX, ALS-74ALSXXX, High-Speed CMOS-74HCXXX, High-Speed CMOS/TTL-74HCTXXX, Advanced CMOS/TTL (ACL)-74ACT11XXX, Advanced CMOS (ACL)-74AC11XXX, and both 10K and 100K ECL.

Due to the great diversity of product families and the different testing requirements and complexity of the product types of each family, Signetics SPD Characterization has designed and built a bench test AC fixture that is specifically designed to address to only the High-speed logic families. It has the advantages of being very versatile, has high bandwidth capability ($\geqslant$750MHz), is 50Ω system compatible, and is manually programmable for the input static voltages. This provides the ability to have one fixture that addresses many product types across families. The extent of this versatility is explained in the following Application Note. The families that this fixture is intended to support are: FAST, ALS, ACL, 10K ECL, and 100K ECL (Note: This fixture is compatible with any 500Ω pull-down load.)

THEORY OF OPERATION

There are several key points in testing the faster edge-rate logic families. They are:

- Very good by-passing and decoupling (they are different).
- Large ground and V_{CC} planes
- Low-impedance signal lines (i.e., 50Ω)
- Signal lines that are uniform in impedance over frequency
- Signal lines must have high bandwidth (> 500MHz)
- Low-inductance paths for the DUT leads, including V_{CC} and GND
- Output AC load close to the DUT

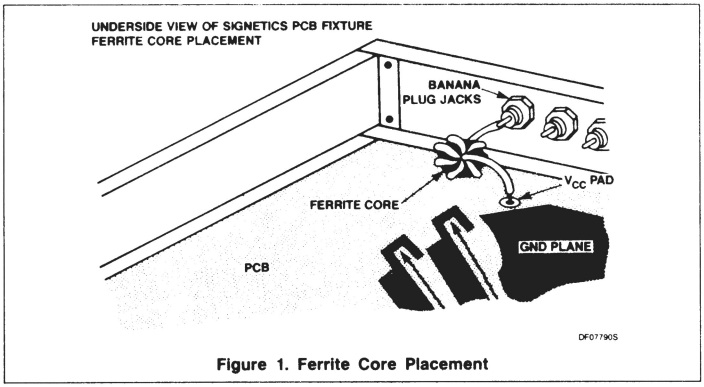


Figure 1. Ferrite Core Placement

- Measurement point close to the DUT
- Avoidance of ground loops (especially on inputs at DC levels)

Also of concern to the test engineer and the manager are:

- Versatility and/or ease of use (there are tradeoffs)
- Cost
- The number of fixtures needed to support products

Each of these concerns have merit and must be understood by the user of these logic families if valid and correlatable results are to be found.

V_{CC} and GND

The secret in V_{CC} and GND use in fixturing is to do the things that reduce the noise that can: 1) get to your part, and 2) come from your part. This is done by reducing the noise of the V_{CC} as it arrives to the fixture, by judicious application of frequency dependant by-passing at the DUT V_{CC} pin to GND and reducing inductance from the V_{CC} and GND pins of the DUT to the point where good contact of the by-passing and V_{CC} and GND planes occur. All of these are techniques used in good RF and microwave board design. By reducing parasitic inductances and cleaning up any sources of noise, good signal integrity is better maintained.

These points are evident in the fixture Signetics has designed. Part of the noise reduction of the power supply as it arrives is done by by-passing the power supply at its terminals. The power is then brought to the fixture via banana cables, (as short as possible), to jacks on the chassis of the fixture. An 18 gauge wire, attached to the jack, is wrapped through a $^{3}/_{4}$ inch ferrite core 8 – 12 times for decoupling of any spikes. (Details of the cores used are included in the parts list.) This acts as a Low-pass filter. The wire is then soldered to the bottom of the PC board onto the large V_{CC} plane that narrows to the V_{CC} bus running between the pins of the DUT. See Figures 1 and 2 for detail.

Triangle-shaped, the V_{CC} plane provides a Low inductive path for the V_{CC} to the DUT pin. See Figure 2 for the board layouts. The V_{CC} bus from this plane travels down between the DUT pins to that connection. This is so connection to the V_{CC} bus is easy and very short. The DUT may have V_{CC} located on any pin with this configuration. The pin is connected to the V_{CC} bus by soldering small copper braid or similar Low-inductance wire capable of carrying the current for the device, see Figure 3.

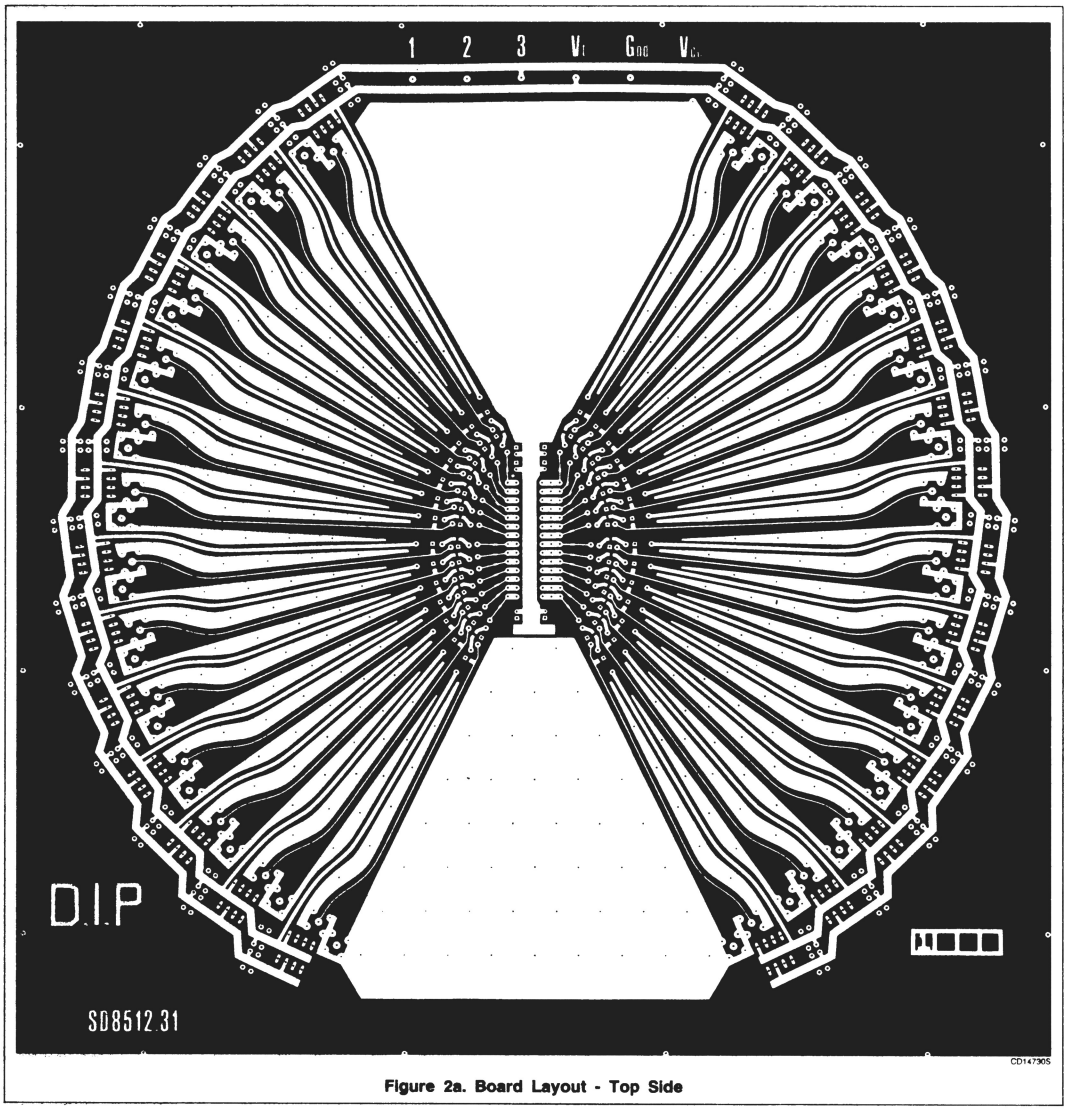


Figure 2a. Board Layout - Top Side

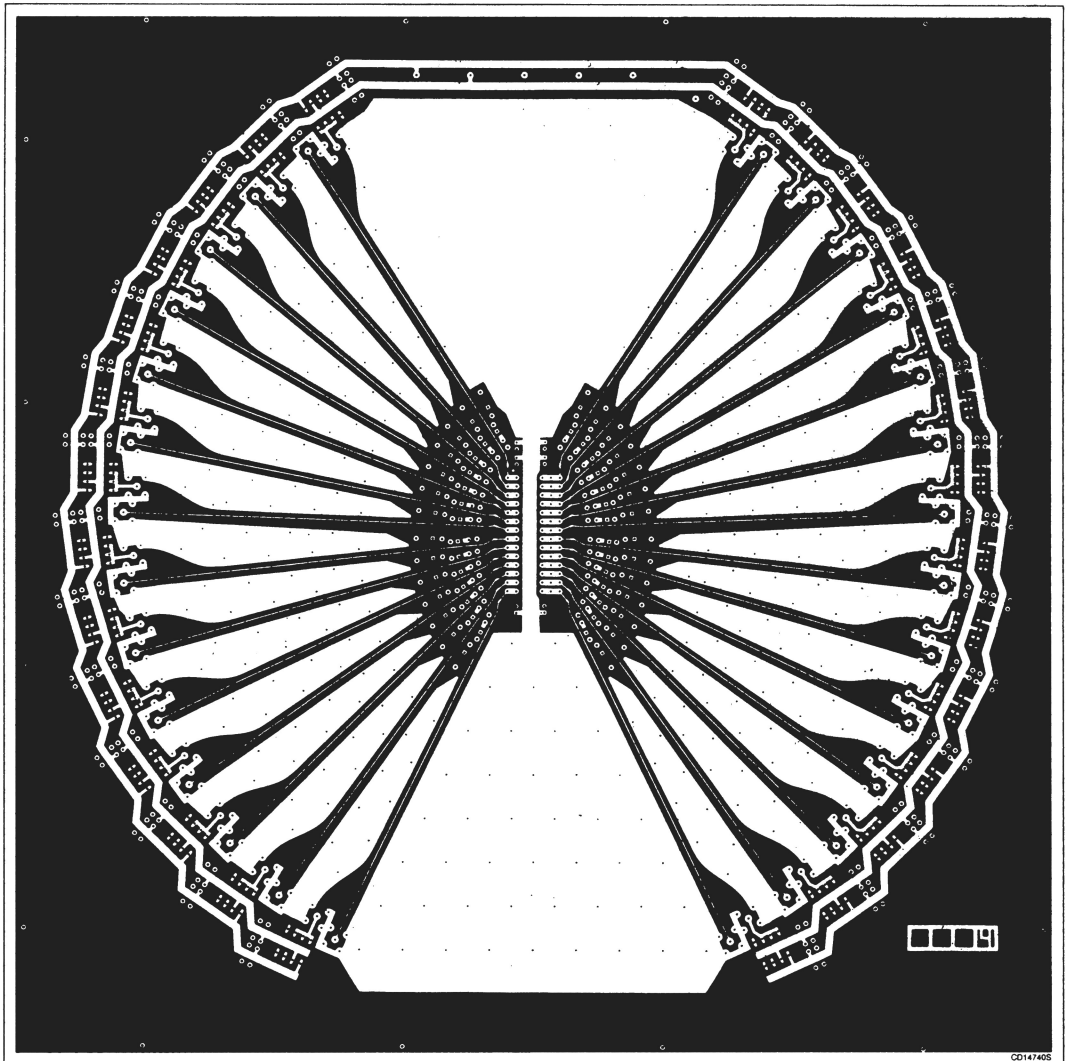


Figure 2b. Board Layout - Bottom Side

On the opposite side of the top layer of the board is a triangle-shaped ground plane. Ground planes are also located on the bottom layer of the board in the same places as the V_{CC} and ground planes of the top layer. Since this fixture is laid out for 50Ω stripline, layers 2 and 3 are almost total ground plane, with holes in them for feed-throughs and components. Also found between the signal lines, on the top and bottom layers, are ground plane "fingers" that are connected to all 4 layers by plated-through holes. This provides good separation of the signal lines resulting in lower cross-talk.

The bottom layer ground plane consists of two triangle-shaped planes connected by a bus strip that runs between the DUT pins. This was done for 3 reasons: First, this allows connection of any ground pin of the DUT to the ground, regardless of location; like the V_{CC} connection on the top layer. Second, it allows the connection of the by-pass capacitors from the V_{CC} pin to the ground with the shortest possible lead length. Characterization uses typically 2 or 3 ceramic chip capacitors and 1 or 2 dipped tantalum capacitors (35V) to by-pass the V_{CC} pin. It is important to keep the dipped tantalum capacitor's leads as short as possible to reduce series inductance. The recommended values of capacitors are: 100pf, .01μf, .1μf. and 10μf. We have found at times, the need to adjust these values depending upon the product type and its performance. Some noise sensitive circuits need more by-passing in the lower and extreme higher values of capacitance. And third, the connection of the two planes eliminates possible ground loops and the feed-throughs create a ground mesh and give an excellent ground plane for the circuit. Figure 3 illustrates the by-pass connections.

BY-PASS AND DECOUPLING

It is important to understand the difference between decoupling, as with the ferrite core, and by-passing, as with capacitors. Decoupling occurs as High-frequency signals are removed by saturation of the ferrite core. This prevents "noise" that may be on the V_{CC} power supply from getting on the V_{CC} plane. The action of the by-passing capacitors is to: 1) "pass" any non-DC signals that occur on the V_{CC} (due to the part's operation) to ground, and 2) be able to provide the "instantaneous" current demands of the part as it switches.

The various values of capacitors are intended to provide a Low-impedance path at all operating frequencies. Since real-world capacitors have resonance points at a given frequency, depending upon their value and type of capacitor (and actually turn inductive above the resonance point), using different values that have different resonance points allows an across-frequency Low-impedance path for V_{CC} noise.

An important point in the use of by-pass capacitors is the minimization of lead length. Lead length represents inductance; inductance in series with the capacitance. If it is too much, it can cause resonance and oscillation problems with the part and/or power supplies and nullify the benefit of the capacitors. It also plays a major part in inhibiting the effect of the "instantaneous" current response needed by the part from the by-pass capacitors. It actually can cause the ground of the device to track the change in current to the degree of the lead inductance. The lower the inductance, the lower the "ground bounce" effect. Hence, short or no lead lengths on capacitors are needed to help prevent the effects of ground bounce.

SIGNAL LINES

A signal line is defined as a line that carries the input stimulus, either DC or AC, or output response, to or from the device. Since these signals are measured and determine the data which characterizes the part, it is critical that they are of the highest integrity and represent, as far as physically possible, the action of the part; not the nuances of the fixture. To achieve this, the line must not be able to change the signal over the measureable frequencies of the device, nor affect the delay of the part.

The fixture as designed, has 50Ω signal lines determined by a stripline layout method. The 50Ω value was selected for several reasons: 1) the 50Ω value matches impedance with the pulse generators that are used as input stimulus. 2) The output loads specified for this fixture are either a 500Ω pull-down or a 50Ω pull-down (ECL), in parallel with a capacitive load. This allows the 50Ω signal line to be terminated into this load for either a 10:1 or a 1:1 match. 3) A Low-impedance line will have better characteristics with regards to cross-talk and resisting external noise.

There are two types of signal lines on this fixture: input and output; both of which are 50Ω transmission lines. The input line is on the top side of the board and is always terminated in 50Ω. It is connected to the DUT via a .3" jumper, Jumper #1 for input. When this jumper is installed, the DUT pin is available only as an input. To allow this line to be used as an output, a .1" jumper, Jumper #1 for output, is used instead of the .3" jumper. This connects the DUT pin to the AC load when the DUP pin is an output. See Figure 5.

The output signal line can be dedicated two different ways. The first method, used for ECL, is to leave shorted the 50Ω trace and have it run directly into the SMB connector into the 50Ω sampling system. The second method is to cut the trace at the DUT pin and solder the 450Ω chip resistor, R1, across the cut. This, combined with the 50Ω scope, then appears to the part as either a 500Ω probe for the input signal or the 500Ω output AC load for the output signal.

The signal lines are equal length and therefore do not introduce any extraneous delay from pin to pin. We also characterized the impedance of the lines over frequency to ensure minimal distortion over the frequency range and any effective change in propagation delay caused by the relationship of inductance and group delay, see Ap Note 202. Figure 4 illustrates the frequency response of the signal lines in impedance.

This is considered to be high bandwith and encompasses the frequency range exhibited by ALS, ACL, ELC, and FAST logic families.

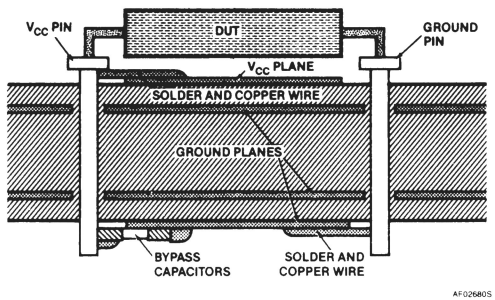


Figure 3. Decoupling Connections

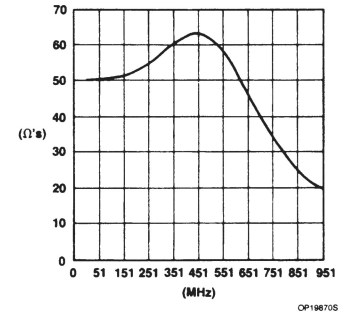


Figure 4. Signal Line Frequency Response

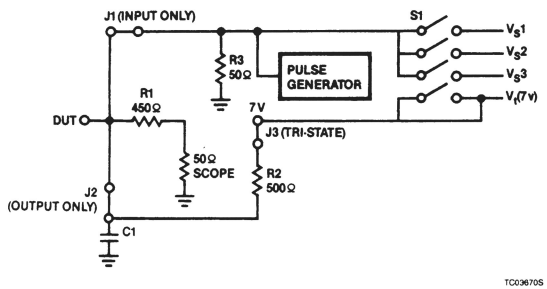


Figure 5. Signetics PCB Fixture Schemetic

LOADING

The explanation of the two types of AC loads that may be used will be covered in two parts. First the ALS, ACL, and FAST implementation will be discussed, then the ECL implementation.

ALS. ACL, and FAST Implementation

The FAST, ALS, and ACL product families AC load is specified as a 50pF capacitor and a 500Ω resistor in parallel. This load has the advantage of being adaptable to both a High-impedance (A.T.E.) or a Low-impedance (bench) measurement environment. The Signetics fixture uses a Low-impedance environment primarily for two reasons. The first reason is that experience of the last 5 years has told us that High-impedance probes represent a reliability concern and can introduce hard to detect errors into the waveform. The second reason being that most suppliers of these technologies provide data based upon the Low-impedance approach and most large users of these products do so as well. This also allows the fixture to be used for ECL testing since that product uses a totally 50Ω environment. Figure 5 illustrates how this test fixture implements the 50pF/500Ω load schematically.

The fixture was laid out to present the load as close as possible to the device, and yet allow for flexibility in deciding if a certain pin is an output or an input. This distance is critical due to its inductive effect upon ground bounce phenomena. *It is acknowledged here that a fixture dedicated to a single device type without jumpers, and therefore placing the load virtually on the pin of the device, would show the ground bounce phenomena for simultaneous switching to be less than that of this fixture. However, this fixture can be so dedicated by not using the pads as provided, but rather by using the ground bus, like the by-pass capacitors used. The flexibility of this fixture substantially reduces the cost of fixturing for these families. Studies on simultaneous switching with this fixture have shown dramatically favorable results to previous fixtures. Those studies continue. For work other than that of simultaneous switching, there will be no appreciable difference with a dedicated fixture.*

As illustrated in Figure 5, the load is shared with the 50Ω input of the measurement system; a 50Ω sampling oscilloscope. The 450Ω resistor: R1, is soldered to the socket pin of the device and is in series with the 50Ω input of the scope. Figure 6 illustrates this on the board layout of one input/output pin. This allows virtually a probe tip on the device pin. The load capacitor: C1, is a 33pF ceramic chip capacitor. This is added to the measured value of 17pF of board capacitance, achieving the 50pF value specified for the load. The distance from the pin to the capacitor is .5 inches and is adequate for the testing of these product families.

For testing 3-State parameters, the 500Ω resistor: R2, is connected to it's pull-up supply. V_t via a .3" jumper: Jumper #2. The V_t supply is bussed to each pin and may or may not be connected with that jumper. See Figures 5 and 6.

ECL Implementation

When testing ECL product, the 450Ω resistor: R1, is not used, Rather, this point is left shorted together in the construction process. Also for ECL, the load chip capacitor: C1, the tri-state pull-up resistor: R2, the 50Ω terminator: R3, and the "output only" jumper: Jumper #1, are not used. The input signal travels down the input path, is jumpered using the "input only" (Jumper #1), goes to the device, travels out the output path (left shorted, no R1), and proceeds to the scope. When the signal is an output, the "input only" jumper: Jumper #1, is removed and a 50Ω terminator is connected to the SMB connector as the load or the 50Ω input of the scope. See Figure 7.

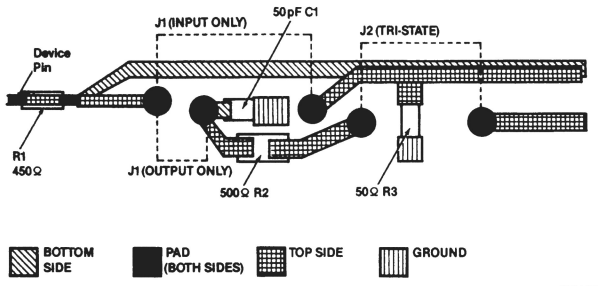


Figure 6. Signetics Fixture - Board

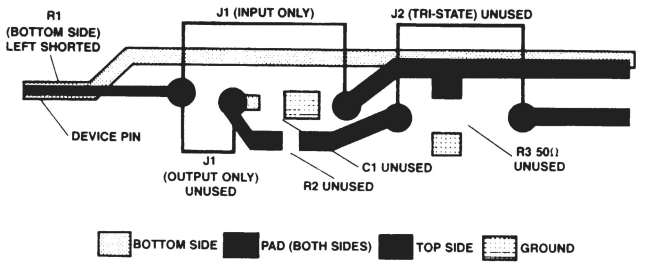


Figure 7. ECL Configuration

INPUT STIMULUS AND MEASUREMENT

When the input is not used for a signal input, the line may be switched to one of three voltage sources: V_S 1 through V_S 3, by the use of a DIP switch on each pin. It may also be left open and then the 50Ω pull-down resistor: R1, pulls the line to ground and can be used as a hard low level. See Figure 5. These voltage levels are brought in from external supplies through banana connectors like V_{CC}. This scheme eliminates excessive cabling to each input to provide the static input levels and thereby reduces parasitic inductances and cross-talk. Each of the 3 busses and the V_t bus all have places for by-pass capacitors in the event of noise on the static levels. Figure 8 illustrates the DIP switch and SMB connectors and how they control the input stimulus and output measurement.

As stated previously, the measurements are made with 50Ω sampling systems. The connections to these systems are made via SMB connectors. This was chosen since it is compatible with SMC; it is push-on, it is small for easy configuration, and it is capable of high bandwidth operation. Figure 8 illustrates where the connections are made, where the pulse generators connect to the input and an SMB connector. Since the 450Ω resistor: R1, is soldered directly to the pin of the device, the actual probe tip is at that point. See Figure 6. This has the advantage of eliminating any distance from the device to the probe tip, thus guaranteeing accurate results.

VERSATILITY AND COST

At some point, there is a choice between the most technically attractive options and the cost of options. This fixture has been primarily designed to optimize the cost effectiveness of test fixturing yet yielding a technically sound tool. To do this, a compromise has been made between the ease of use and the versatility.

In the construction of the fixture, a choice is made as to where the V_{CC} and GND pins are to be located. This then dedicates this particular fixture to part types with this V_{CC} and GND configurations. This is alos done with a dedicated fixture. However, on a dedicated fixture, the pins are individually constructed to be either an input or an output, and in so doing, the fixture is usable for 1-to-4 devices. The Signetics fixture, once dedicated to a particular V_{CC} and GND configuration, is built up to have both input and output components on all signal pins. The selection of which pin is an output or an input is made by inserting the appropriate jumper, See Figures 5 and 6. The same applies in doing tri-state testing. The tradeoff here is that it would probably take less time to setup the dedicated fixture than the Signetics fixture. To help compensate for that tradeoff, we have the three Vs supplies that may be switched into any pin to provide input static levels and eliminate the need to bus input High or Low levels by external cabling. For the user that means the only connections being made to the fixture are:

- the V_{CC} (banana jack)
- the (GND) (banana jack): this is the common ground of all input supplies.
- the V_S 1, V_S 2, and V_S 3 supplies (banana jack): these may be any voltage and are switchable. Signetics connects programmable supplies to these connectors.
- the V_t supply (banana jack): this is the tri-state pull-up voltage and is permanently connected to the bus to each pin. It is selectable by Jumper #2, see Figures 5 and 6. For FAST and ALS products this is 7V. For ACL products this is $V_{CC} \times 2$ and it is not used for ECL applications.
- Input Stimulus (inside SMB connector: this is found on every input/output pin. More than one pin may be used in this manner. **CAUTION:** When using this connector as an input stimulus, make sure V_S 1 – 3 are disconnected. This will short the power supplies to the generator if they are not disconnected.
- Output Measurement or Scope Connection (outside SMB connector: this is also found on every input/output pin. More than one pin may be used in this manner. Remember, if this pin is not connected to a scope and is an output, a 50Ω resistor must be connected here to ground to complete the 50Ω resistive load. Signetics has constructed 50Ω load by soldering a high-quality (High-frequency) 50Ω resistor inside a female SMB cable connector. See Figure 9.

CAUTION: V_S 1,2 and 3 are all on the same DIP switch. Since they connect to the same bus per pin, **ONLY ONE SUPPLY MAY BE CONNECTED AT ONE TIME**, Otherwise, this will result in a short between power supplies connected.

With these 6 connections, the fixture is capable of testing the product lines as mentioned.

The cost of this fixture ranges from 550 per fixture, dedicated to a 20-pin device in quantities of 1 – 10, to as low as 385 per fixture of the same type in quantities over 100. This is not substantially higher than the cost of a dedicated fixture; which is estimated at 200 – 500. The factor to consider would be the quantity of fixtures for the number of products to be tested. To have a dedicated fixture for every 2 – 3 product types versus a "universal" test fixture for 20 – 30 product types is worth considering from a cost standpoint.

Included in Appendix 1 is the parts list for this fixture and the supplies used by Signetics. This in no way constitutes Signetics endorsements of these suppliers and the customer may select their own supplier if they so desire. This fixture is offerd to the public to duplicate and use within their own environments. Signetics will not provide any materials but will allow the manufacturers of the board and materials to build and/or supply for any requesting party. Pricing and availability are left to the vendors and Signetics has no control over those issues. The intent is to provide something for users of High-speed logic that has been proven and tested in a true High-speed use, and provide a characterization of these products prior to their introduction to the market place.

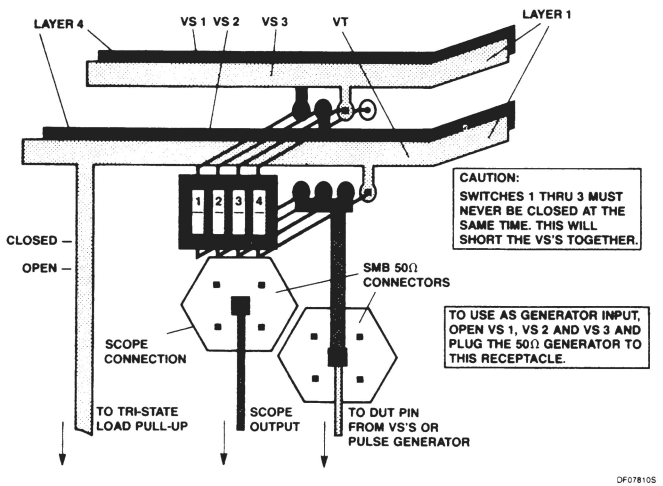

LAYER 4
VS 1 VS 2
VS 3
VT
LAYER 1
CAUTION:
SWITCHES 1 THRU 3 MUST NEVER BE CLOSED AT THE SAME TIME. THIS WILL SHORT THE VS'S TOGETHER.
1 2 3 4
CLOSED
OPEN
SMB 50Ω CONNECTORS
TO USE AS GENERATOR INPUT, OPEN VS 1, VS 2 AND VS 3 AND PLUG THE 50Ω GENERATOR TO THIS RECEPTACLE.
SCOPE CONNECTION
TO TRI-STATE LOAD PULL-UP
SCOPE OUTPUT
TO DUT PIN FROM VS'S OR PULSE GENERATOR
DF07810S

Figure 8. DIP Switch Connections for V_s 1, V_s 2, V_s 3, and V_t and the SMB Connectors for Input Signals and Output Measurement

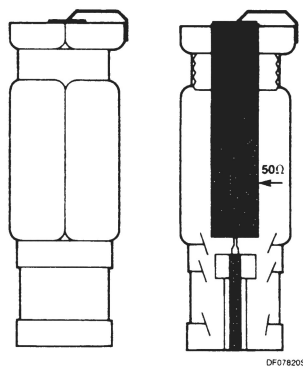


Figure 9. 50Ω Load Resistors Using Output Pin SMB Cable Connectors

APPENDIX I — Component and Vendor List

1. Printed circuit mother board
   - SO and SOL #SD8512.28
   - DIP #SD8512.31
   - Requirement: 1 per part configuration
   - Supplier: Prototype and Production Circuits
     8040 South 1444 West
     West Jordan, UT 84084
     (801) 566-5431

2. SO and SOL sockets

# PINS	PART #
14	001-014
16	001-016
16L	001-116
20	001-120
24	001-124
28	001-128

   SOIC through-hole socket
   Requirement: 1 per board
   Supplier: Surface Mount Devices, Inc.
   PO Box 16818
   Stamford, CT 06903
   (203) 322-8290

3. L$G-1AG14-1 Socket Terminal Pins
   For DIP boards — number of pins equal to the part pin count times by (7) seven.
   $24 \times 7 = 168$
   For SO and SOL boards — number of pins equal to the part pins count times by (5) five.
   $24 \times 5 = 120$

4. Shorting Blocks (Jumpers)
   - 0.3 inch 8136-475G1 Requirement: 1 per pin
   - 0.1 inch 8136-651P2 Requirement: 1 per pin
   - Supplier: Augat

5. Chip Resistors
   - 50Ω 1% CRCW 1210 Requirement: 1 per pin
   - 450Ω 1% CRCW 1206 Requirement: 1 per pin
   - 500Ω 1% CRCW 1206 Requirement: 1 per pin
   - Supplier: Dale Electronics, Inc.
     2300 Riverside Blvd.
     Norfolk, Nebraska 68701
     (402) 371-0080

6. Chip Capacitors
   Ceramic Part #
   - 33pF 500R15N330JP Requirement: 1 per bin
   - 15pF 500R15N150JP4 Requirement: 1 per board
   - 0.015μF 500S41W103KP4 Requirement: 1 per board
   - 0.1μF 500S41W104KP4 Requirement: 1 per board
   - Supplier: Johanson Dielectrics

7. Dipped Tantalum
   Ceramic Part #
   - 10μF 106K025NLF Requirement: 1 per board
   - 47μF 476K020WLG Requirement: 1 per board
   - Supplier: Mallory

8. Ferrite Core
   T80-1 Requirement: 1 per board
   Supplier: Amidon Associates
   12033 Otsego Street
   North Hollywood, CA 91607
   (818) 760-4429

9. Mounting Screw
   4-40 × ¼ Phillips pan head machine screw Requirement: 16 per board.
   Supplier: Bonneville Industry Supply Co.
   45 South 1500 West
   Orem, UT
   (801) 225-7770

10. Banana Plug Jack

H.H. Smith Type		Order #	Requirement
White	1509-101	28F1178	6/board-color your choice
Red	1509-102	35F870	6/board-color your choice
Black	1509-103	35F869	6/board-color your choice
Green	1509-104	28F1179	6/board-color your choice
Blue	1509-105	28F1180	6/board-color your choice
Yellow	1509-107	28F1182	6/board-color your choice

   Supplier: Newark Electronics

11. Switch
   76PSB04 4-bit side actuated piano DIP Requirement: 1 per pin
   Supplier: Grayhill Co.

12. Connectors — Snap-on SMB
   51-051-0000-220 Straight jack receptacle Requirement: 2 per pin
   Supplier: Sealectro

13. Mounting frame
   Signetics number CB-1.0 Requirement: 1 per test fixture
   Supplier: Electronic Chassis Corp.
   468 North 1200 West
   Lindon, UT 84062
   (801) 785-9113

14. Hook-up wire
   No. 18/20 gauge Teflon coated — about 24 inches per test fixture.

The following components may be needed in use of the test fixtures but are not part of the test fixtures.

61-001-0000-89	50Ω terminator plug	As required or hand-built with 50Ω resistor and 51-007-0000
51-007-0000	Straight cable clamp type	As required
51-083-0000-222	"T" adaptor J-J-J	As required
51-085-0000	"T" adaptor J-P-J	As required
51-072-0000	Adaptor J-J	As required
51-073-0000	Adaptor P-P	As required
51-001-0020	Shorting plug	As required
61-002-0000-89	50Ω terminator jack	As required

Supplier: Sealectro Corp
(415) 965-1212

APPENDIX II — Construction Hints

A suggested order of assembly is as follows:

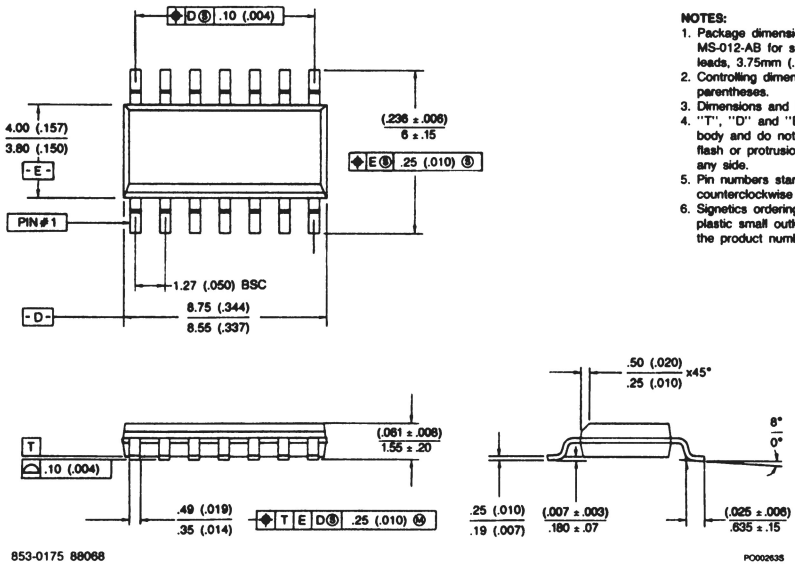
1. Cut traces for 450Ω resistor. (Not needed for ECL)
2. Install SMB Connectors. Elevate base from board 0.05".
3. Install DIP Switches. Note: Numbers on switches may not correlate to V_S supply numbers.
4. Install Augat socket pin.
5. Install load/termination resistors and capacitors.
6. Strap V_{CC} and GND pins to appropriate bus strips.
7. Install bypass capacitors.
8. Clean flux off of board and components.
9. Check for lead to frame shorts on PLCC board. (Not discussed in App Note.)
10. Install banana jacks on frame.
11. Attach board to frame with ¼ Phillips pan head machine screws.
12. Wrap wire 8 – 12 times around ferrite core. Leave enough wire to connect to frame and board. See Figure 1.
13. Connect V_{CC}, GND, and voltage supplies from banana jacks to board.
14. Remove all remaining flux. Keep "flux-off" from banana jacks.

Hints on construction:

- A 0.05" shim that fits under the SMB connector base helps elevate it during construction.
- Mount the SMB connector with flat side out rather that point side out. See Figure 8.
- Solder Augat socket pins in with a part inserted to hold the pins steady.
- "Piano DIP" switches have the numbers reversed from the Board notation. Taping a new number on the board designations will help match the switches.
- Hint for solder chip components: apply a small amount of solder on one side of the pads on the board.
- Keep DIP switches and SMB connectors spaced as far away from each other as the holes will permit, i.e., push the SMBs in and the DIP switches out.

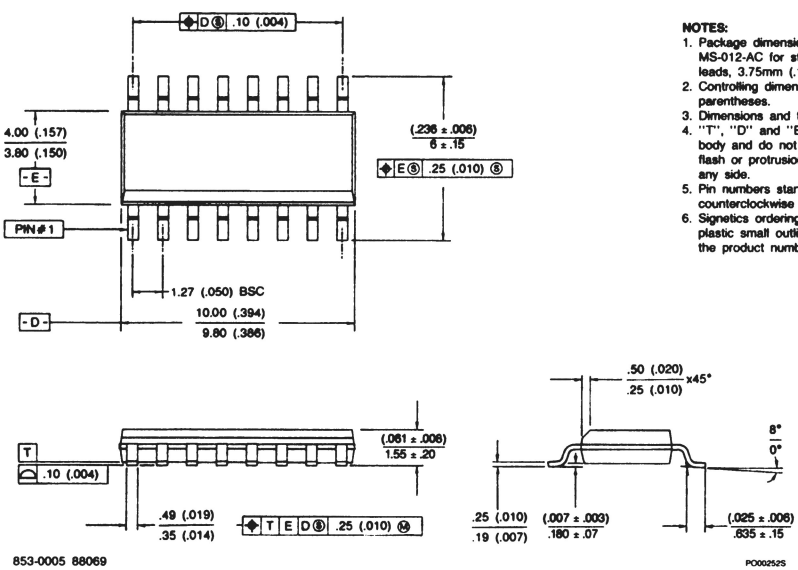
Section 7
Packaging Information

14-PIN PLASTIC SO



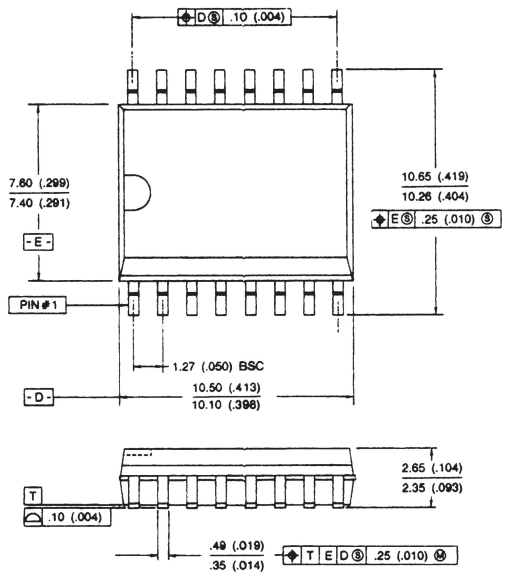
NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SO

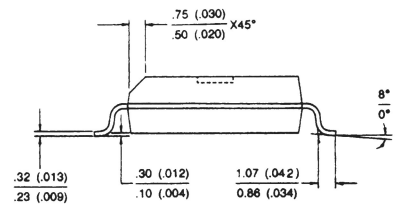


NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

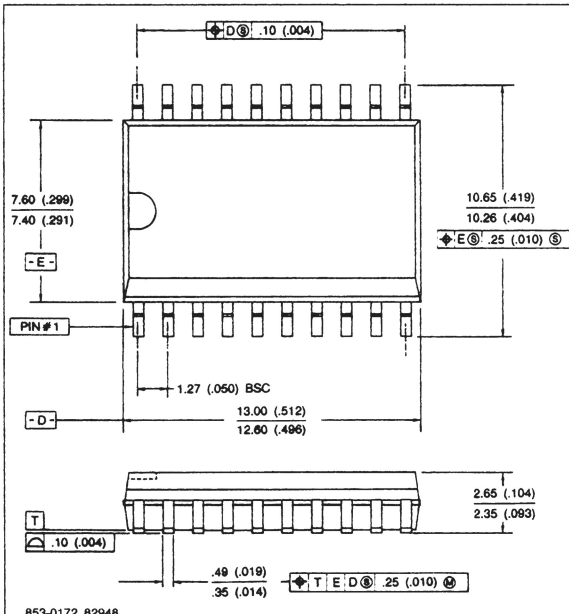
16-PIN PLASTIC SOL



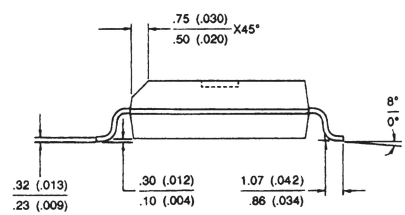
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



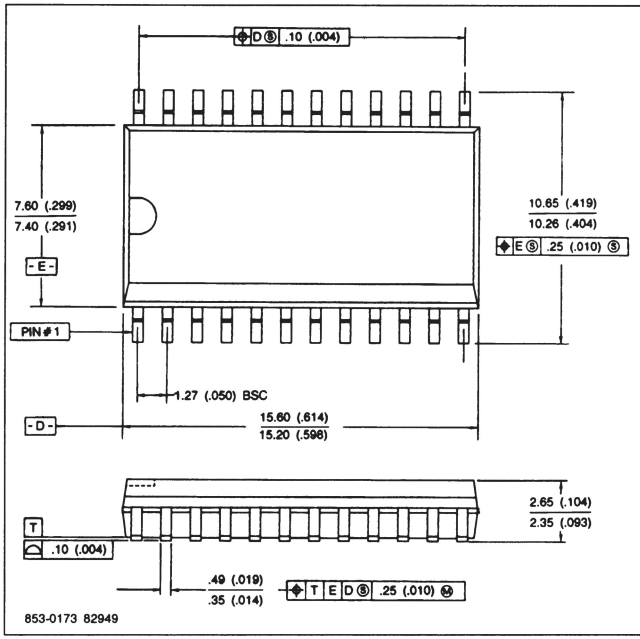
20-PIN PLASTIC SOL

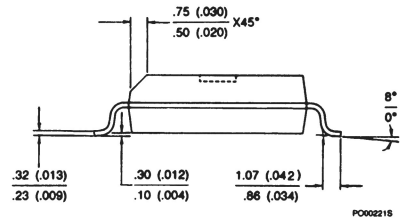


NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



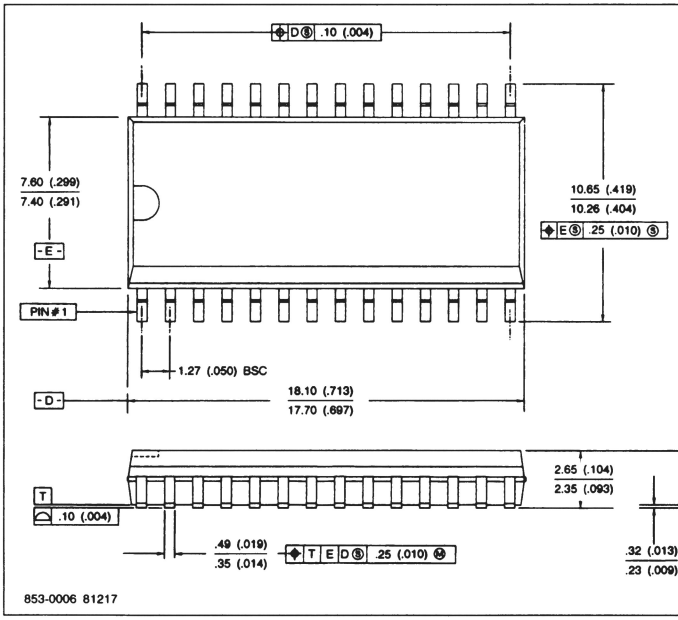
24-PIN PLASTIC SOL

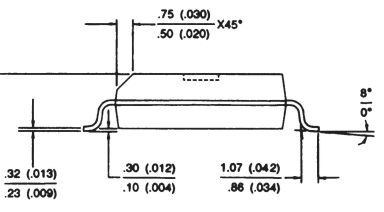




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

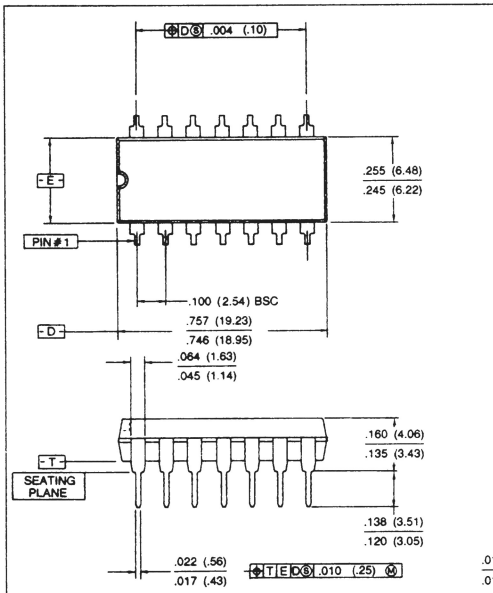
28-PIN PLASTIC SOL





NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

14-PIN PLASTIC DIP

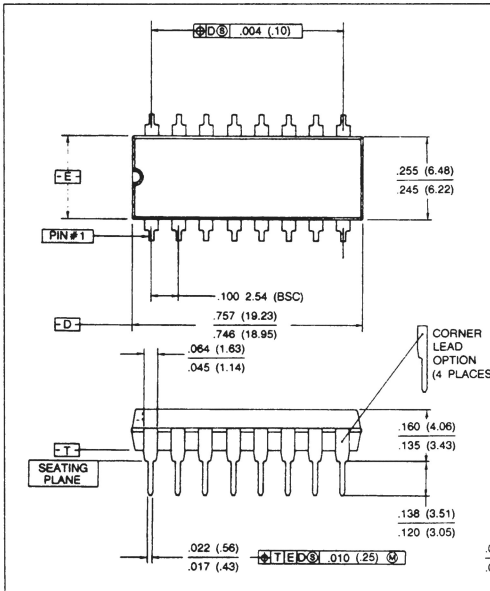


853-0405 81231

PO00330S

NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

16-PIN PLASTIC DIP

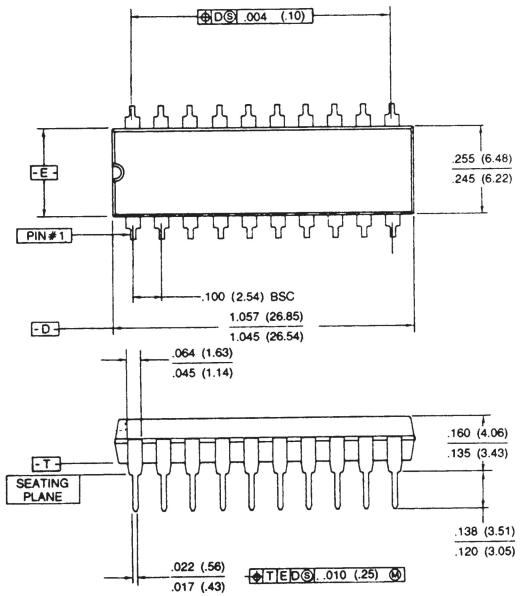


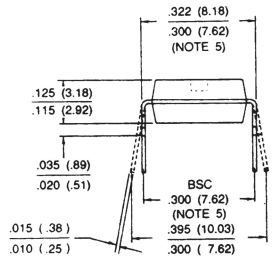
853-0406 81232

PO00280S

NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

20-PIN PLASTIC DIP



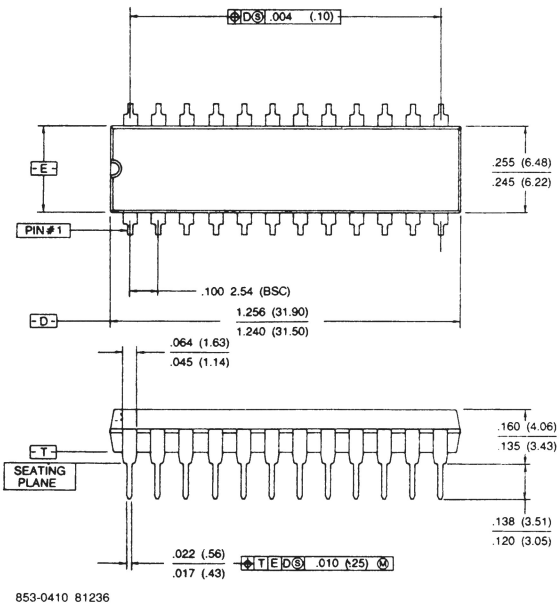


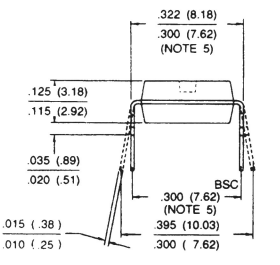
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0408 81234

PO00290S

24-PIN PLASTIC DIP



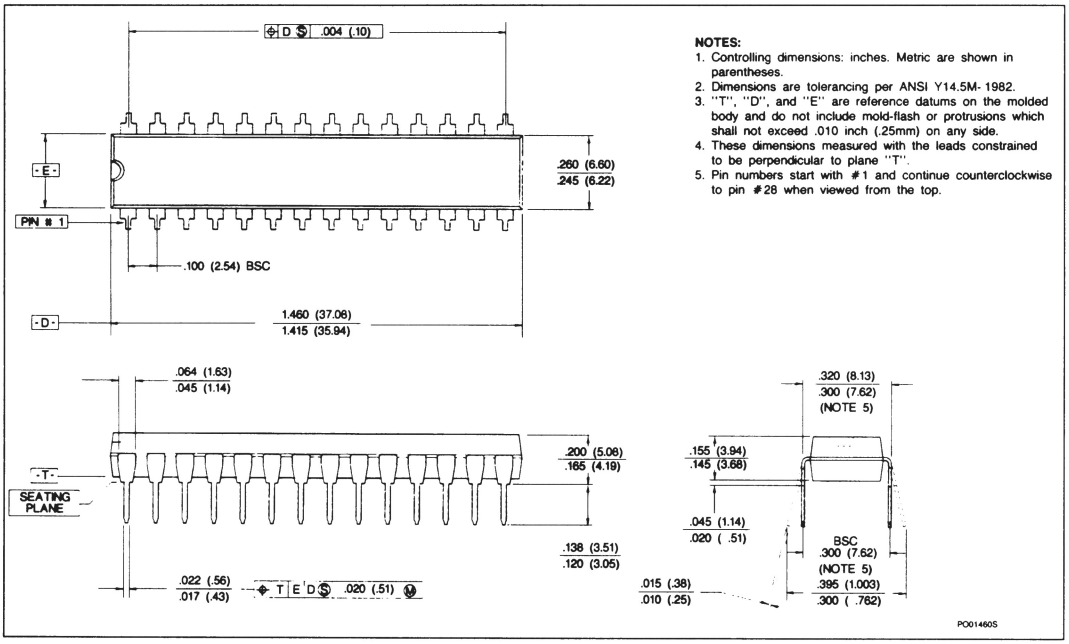


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AR for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0410 81236

PO00320S

28-PIN PLASTIC SKINNY DIP



NOTES:

1. Controlling dimensions: inches. Metric are shown in parentheses.
2. Dimensions are tolerancing per ANSI Y14.5M- 1982.
3. "T", "D", and "E" are reference datums on the molded body and do not include mold-flash or protrusions which shall not exceed .010 inch (.25mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane "T".
5. Pin numbers start with #1 and continue counterclockwise to pin #28 when viewed from the top.

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

NOTES

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages III to VIII.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**not yet issued**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
Supplement to IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** Bipolar, MOS
IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	**SC01**	**Diodes** High-voltage tripler units
S2a	**SC02***	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04***	**Small-signal transistors**
S4a	**SC05***	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07***	**Small-signal field-effect transistors**
S6	**SC08***	**RF power transistors**
	SC09*	**RF power modules**
S7	**SC10***	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12***	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14***	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T8	**DC01**	**Colour display systems**
T16	**DC02***	**Monochrome tubes and deflection units**
C2	**DC03***	**Television tuners, coaxial aerial input assemblies**
C3	**DC04***	**Loudspeakers**
C20	**DC05***	**Wire-wound components for TVs and monitors**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
C14	**PA01**	**Electrolytic capacitors; solid and non-solid**
C11	**PA02***	**Varistors, thermistors and sensors**
C12	**PA03***	**Potentiometers, encoders and switches**
C7	**PA04***	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08***	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T1	*	Power tubes for RF heating and communications
T2a	*	Transmitting tubes for communications, glass types
T2b	*	Transmitting tubes for communications, ceramic types
T3	PC01**	High-power klystrons
T4	*	Magnetrons for microwave heating
T5	PC02**	Cathode-ray tubes
T6	PC03**	Geiger-Müller tubes
T9	PC04**	Photo and electron multipliers
T10	PC05**	Plumbicon camera tubes and accessories
T11	PC06**	Microwave diodes and sub-assemblies
T12	PC07**	Vidicon and Newvicon camera tubes and deflection units
T13	PC08	Image intensifiers and infrared detectors
T15	PC09**	Dry reed switches
C8	PC10	Variable mains transformers; annular fixed transformers

* These handbooks will not be reissued.
** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 C5	MA01*	**Soft Ferrites**
C16	MA02**	**Permanent magnet materials**
C19	MA03**	**Piezoelectric ceramics**

* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

** Not yet issued with the new code in this series of handbooks.

Philips Components – a worldwide Group of Companies

Argentina: PHILIPS ARGENTINA S.A., Div. Components, Vedia 3892, 1430 BUENOS AIRES, Tel. (01) 541 - 7141 to 7747.
Australia: PHILIPS COMPONENTS PTY Ltd, 11 Waltham Street, ARTARMON, N.S.W. 2064, Tel. (02) 439 3322.
Austria: ÖSTERREICHISCHE PHILIPS INDUSTRIE G.m.b.H., UB Bauelemente, Triester Str. 64, 1101 WIEN, Tel. (0222) 60 101-820.
Belgium: N.V. PHILIPS PROF. SYSTEMS – Components Div., 80 Rue Des Deux Gares, B-1070 BRUXELLES, Tel. (02) 525 6111.
Brazil: CONSTANTA-IBRAPE; (Active Devices): Av. Brigadeiro Faria Lima, 1735-SAO PAULO-SP, Tel. (011) 211-2600. CONSTANTA-IBRAPE; (Passive Devices & Materials): Av. Francisco Monteiro, 702 – RIBEIRAO PIRES-SP, Tel. (011) 459-8211.
Canada:

Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. (02) 77 38 16.
Colombia: IND. PHILIPS DE COLOMBIA S.A., c/o IPRELENSO LTD., Cra. 21, No. 56-17, BOGOTA, D.E., Tel. (01) 249 76 24.
Denmark: PHILIPS COMPONENTS A/S, Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. 01-54 11 33.
Finland: PHILIPS COMPONENTS, Sinikalliontie 3, SF-2630 ESPOO HELSINKI 10, Tel. 358-0-50 261.
France: RTC-COMPELEC, 117 Quai du Président Roosevelt, 92134 ISSY-LES-MOULINEAUX Cedex, Tel. (01) 40 93 80 00.
Germany (Fed. Republic): VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
Greece: PHILIPS HELLENIQUE S.A., Components Division, No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01) 48 94 339/48 94 911.
Hong Kong: PHILIPS HONG KONG LTD., Components Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-24 51 21.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Components Dept., Band Box Building, 254-D Dr. Annie Besant Rd., BOMBAY – 400 025, Tel. (022) 493 0311/493 0590.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Components Div., Setiabudi II Building, 6th Fl., Jalan H.R. Rasuna Said (P.O. Box 223/KBY) Kuningan, JAKARTA 12910, Tel. (021) 517 995.
Ireland: PHILIPS ELECTRONICS (IRELAND) LTD., Components Division, Newstead, Clonskeagh, DUBLIN 14, Tel. (01) 69 33 55.
Italy: PHILIPS S.p.A., Philips Components, Piazza IV Novembre 3, I-20124 MILANO, Tel. (02) 6752.1.
Japan: NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. (03) 448-5611.
(IC Products) SIGNETICS JAPAN LTD., 8-7 Sanbancho Chiyoda-ku, TOKYO 102, Tel. (03) 230-1521.
Korea (Republic of): PHILIPS ELECTRONICS (KOREA) LTD., Elcoma Div., Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. (02) 794-5011.
Malaysia: PHILIPS MALAYSIA SDN BHD, Components Div., 3 Jalan SS15/2A SUBANG, 47500 PETALING JAYA, Tel. (03) 734 5511.
Mexico: ELECTRONICA, S.A de C.V., Carr. México-Toluca km. 62.5, TOLUCA, Edo. de México 50140, Tel. Toluca 91 (721) 613-00.
Netherlands: PHILIPS NEDERLAND, Marktgroep Philips Components, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 78 37 49.
New Zealand: PHILIPS NEW ZEALAND LTD., Components Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. (09) 605-914.

Norway: NORSK A/S PHILIPS, Philips Components, Box 1, Manglerud 0612, OSLO, Tel. (02) 68 02 00.
Pakistan: PHILIPS ELECTRICAL CO. OF PAKISTAN LTD., Philips Markaz, M.A. Jinnah Rd., KARACHI-3, Tel. (021) 725772.
Peru: CADESA, Av. Pardo y Aliaga No. 695, 6th Floor, San Isidro, LIMA 27, Tel. (014) 707080.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. (02) 86 89 51 to 59.
Portugal: PHILIPS PORTUGUESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. (019) 68 31 21.
Singapore: PHILIPS PROJECT DEV. (Singapore) PTE LTD., Components Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 350 2000.
Spain: PHILIPS Components, Balmes 22, 08007 BARCELONA, Tel. (03) 301 63 12.
Sweden: PHILIPS Components, A.B., Tegeluddsvägen 1, S-11584 STOCKHOLM, Tel. (0)8-782 10 00.
Switzerland: PHILIPS A.G., Components Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. (01) 488 22 11.
Taiwan: PHILIPS TAIWAN LTD., 150 Tun Hua North Road, P.O. Box 22978, TAIPEI, Taiwan, Tel. (02) 71 20 500.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. (02) 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., Philips Components, Talatpasa Cad. No. 5, 80640 LEVENT/ISTANBUL, Tel. (01) 179 27 70.
United Kingdom: PHILIPS COMPONENTS LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. (01) 580 6633.
United States: AMPEREX ELECTRONIC CORP., 230 Duffy Avenue, P.O. Box 560, HICKSVILLE, L.I.N.Y. 11802, Tel. (516) 931-6200.
(Active Devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Colour picture tubes – Monochrome & Colour Display Tubes) PHILIPS DISPLAY COMPONENTS, 50 Johnston St., SENECA FALLS, N.Y. 13148, Tel. (315) 568-5881.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. (408) 991-2000.
(Passive & Electromech. Dev.) MEPCO/CENTRALAB, INC., 2001 West Blue Heron Blvd, RIVIERA BEACH, Florida 33404, Tel. (305) 881-3200.
Uruguay: LUZILECTRON S.A., Avda Uruguay 1287, P.O. Box 907, MONTEVIDEO, Tel. (02) 985395.
Venezuela: IND. VENEZOLANAS PHILIPS S.A., c/o MAGNETICA S.A., Calle 6, Ed. Las Tres Jotas, App. Post. 78117, CARACAS, Tel. (02) 239 39 31.

For all other countries apply to: Philips Components Division, International Business Relations, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Telex 35000 phtcnl

AS67 © Philips Export B.V. 1989

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands 9398 152 70011

Philips Components

PHILIPS